TIME-DOMAIN EFFECTS OF DIFFERENTIAL PARALLEL AMPLIFIER MISMATCH MEASURED WITH AN EYE DIAGRAM

by

JOSHUA GRAHAM OLSON

B.S., Colorado State University, 2016

A thesis submitted to the Graduate Faculty of the
University of Colorado Colorado Springs
in partial fulfillment of the
requirements for the degree of
Master of Science
Department of Electrical Engineering
2022

This thesis for the Master of Science degree by

Joshua Graham Olson

has been approved for the

Department of Electrical Engineering

by

T.S. Kalkur, Chair

John Lindsey

Heather Song

Date 12/6/2022

Olson, Joshua Graham (M.S. Electrical Engineering)

Time-Domain Effects of Differential Parallel Amplifier Mismatch Measured with Eye Diagram

Thesis directed by Professor T.S. Kalkur

ABSTRACT

The field of electronics in the year 2022 is experiencing greater pushing of frequency and performance limitations more than ever before. This brings along unique signal amplification and processing challenges, in addition to new IC fabrication complications. An increasing number of cases now exist where there is need for multiple ICs, such as amplifiers or analog-to-digital converters, to operate in parallel and with significant weight on timing synchronization. This thesis attempts to characterize, in the time-domain, the effects of mismatch between two parallel amplifiers operating on two individual halves of a differential signal.

A parallel amplifier circuit using BJTs is designed in Spice software and Advanced Design System, operating on a 250MHz differential clock signal. Multiple parameters of the two amplifiers are swept and the output of this differential signal is measured using an eye diagram utility in the ADS software. Correlations between mismatch of collector resistance, beta value, and emitter resistance in the two amplifiers and outputs in the eye diagram - eye height, rise and fall time, signal-to-noise-ratio, logical voltage levels - are characterized and curves fitted to the data.

This thesis finds that mismatch between two parallel amplifiers has substantial and relevant effects on performance and bit clarity (bit error rate) of a differential digital clock signal. These effects have also been found to increase with frequency.

ACKNOWLEDGEMENTS

I would like to first thank Keysight Technologies and my manager, Shane Millburn, for funding and fully supporting my pursuit of an advanced degree. Two of the people most responsible for specifically inspiring my pursuit of further knowledge are my mentor, Bill Duffy, and my father-in-law, Ron Kilgore. My colleague and best friend, Ian Hess, has regularly taken on additional workload over the past three years whenever school demands became urgent. I also want to recognize David Kambich for his advice and support throughout my master's degree. Dr. Kalkur and Dr. Lindsey at UCCS have been extremely patient and willing to answer my relentless questions throughout this thesis.

My parents, Brad and Carol Olson, have been truly unrelenting in their support and praise of every single thing I do. To loosely paraphrase Sir Isaac Newton, if I have been able to accomplish anything noteworthy in my life, it is because I stood on their shoulders.

Finally, I owe an insurmountable debt of gratitude to my incredible wife, Rylie. She has made so many sacrifices over these past three years, and her patience throughout my ongoing battle with procrastination has seemingly known no bounds. Through all the late nights, the extra-long workdays, and the emotional weight that I was inevitably unable to keep my family completely shielded from while pouring myself into this degree and working full-time, Rylie never once stopped supporting me and lifting me up. This thesis was supposed to be completed in May of 2021, two weeks before our first daughter Rayna was due. A year and a half later, with our second child due in May of 2023, there is no way I could be here without the constant support of the most incredible wife in the world. (She doesn't understand it yet, but I truly owe much of my perseverance and lifted spirits to my absolute delight of a daughter, Rayna).

TABLE OF CONTENTS

LIST OF TABLES

TABLE

LIST OF FIGURES

FIGURE

CHAPTER 1 INTRODUCTION

In an era of rapidly increasing data-transfer speed requirements, the demand for higher-frequency integrated circuits is a rising problem in chip design and application. As frequency increases, overall transistor size decreases. The result of smaller and smaller gaps within IC's is a significantly higher probability of seeing random microscopic debris and minute process variations cause dramatic changes in transistor width and, therefore, variations in overall performance. As demands increase for higher frequencies, it is not uncommon to see a differential digital clock configuration for applications such as time-interleaved data converters or digital samplers. A unique case exists where there is need for two individual amplifier chips to be placed in parallel, amplifying two halves of this differential clock signal separately and individually. As a result of process and random variations in the fabrication of each individual amplifier IC, these two amplifiers in parallel can end up amplifying the positive and negative halves of the differential signal differently. It is only with recent, higher frequency technology that this two-amplifier layout is becoming a viable and often necessary solution. Therefore, very little research currently exists to characterize the advantages and disadvantages.

The following thesis will begin with an analysis of existing work related to this topic, identifying common amplifier criteria and previously identified process variations in amplifier IC's. This will be followed by a section outlining the basic criteria that will be used to identify and compare variations at the output of the differential pair. A parallel BJT common-base amplifier is then designed in Spice and Advanced Design System software with design constraints and circuit schematics given. After expected theoretical

input mismatch and output correlations are derived, simulations are performed in Advanced Design System to prove, disapprove, and verify predictions.

1.1 Time-Interleaved Analog-to-Digital Converters

It was previously presented that increases in frequency demands result in a potential need for two amplifiers operating in parallel on a differential line. One example of a similar situation is a time-interleaved analog-to-digital converter, shown in Figure 1.1 below.

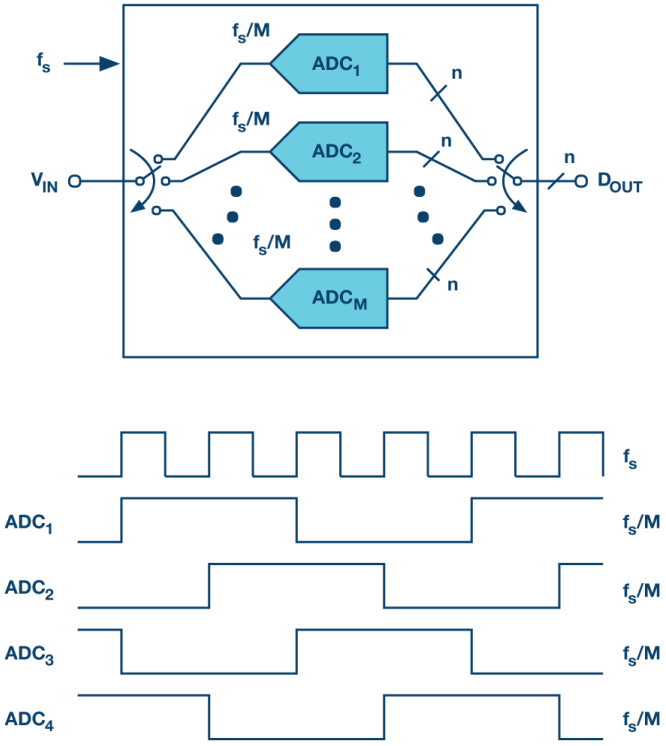

Figure 1.1: Time-Interleaved A/D Converter – Analog Dialogue

This unique ADC configuration arises as a solution to single ADCs that are not fast enough for the desired application. In this case, multiple slower-speed A/D converters are operated “in parallel”, each sampling a separate section of the input signal. This operation relies heavily on a clock signal which is phase-shifted to precisely and periodically section the input signal into individual pieces to be sampled by each ADC.

Time-interleaved A/D converters are highly sensitive to and limited by mismatch between the parallel signal paths, primarily mismatch in “dc offset, gain, or sampling time” (Analog Integrated Circuit Design, 2011). The simulation performed in this thesis is actually quite similar to this case, but slightly more generalized. Instead of analyzing frequency domain mismatch between these A/D converters, this thesis will focus on a two-sided differential line and amplify the two halves separately.

1.2 Amplifiers

In modern electronics, as it’s been for decades, an electrical signal is often times too small (low voltage or power) for the specific application. In an audio system, for example, the music signal from the CD player is far too weak to power speakers and make it loud enough for listening. Here we see one example of the need for the amplifier. The amplifier is one of the most significant semiconductor devices that exists today, used in everything from stereo receivers to biomedical equipment.

1.2.1 Single-Ended Amplifier Basics

A two-port device, the signal at the output port will be a duplicate of the input signal but with increased magnitude in some way, whether it’s voltage, current, or power. All amplifiers are subject to various tradeoffs, much like most electronic devices, with two of the most common being gain and noise. As the operating frequency of the amplifier increases, many new challenges and tradeoffs are introduced. There exist many real-world applications that require reasonably high frequencies while still desiring significantly high gain from the amplifier. Many of these situations involve a differential signal to decrease noise in the system, which leads to discussion on the differential

amplifier in the next section. Figure 1.1 below shows the basic circuit diagram for a MOSFET amplifier.

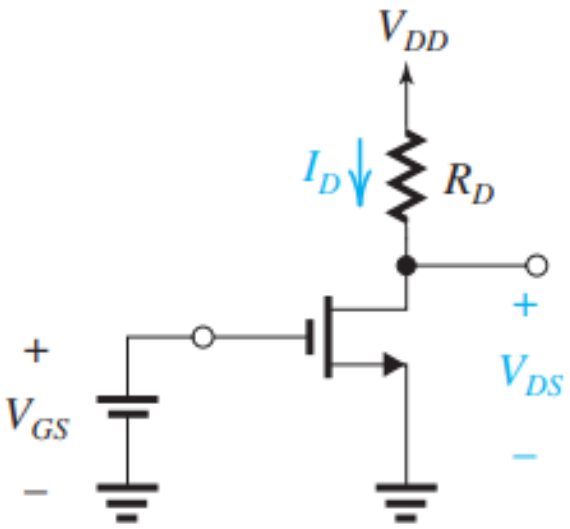

Figure 1.2: MOSFET Amplifier - Sedra and Smith

1.2.2 Differential Amplifiers

When reduction of noise is most important, it is often advisable to use a differential amplifier in place of a single-ended amplifier. A differential amplifier setup is significantly less sensitive to interference from nearby devices and to noise in general. This is a result of the fact that a differential amplifier is capable of cancelling out any noise or extraneous signal that exists on both sides of the amplifier (Sedra, Smith, Carusone, & Gaudet, 2020). Generally, a differential amplifier exists on a single IC. With modern high frequency and high gain demands, however, there is a potential need for two individual single-ended amplifiers with relatively high performance two operate “in parallel” in a differential configuration. The experimental section of this thesis will attempt to outline and prove the viability of and problems with this configuration. Figure 1.2 below shows a simple circuit layout for a differential MOSFET amplifier.

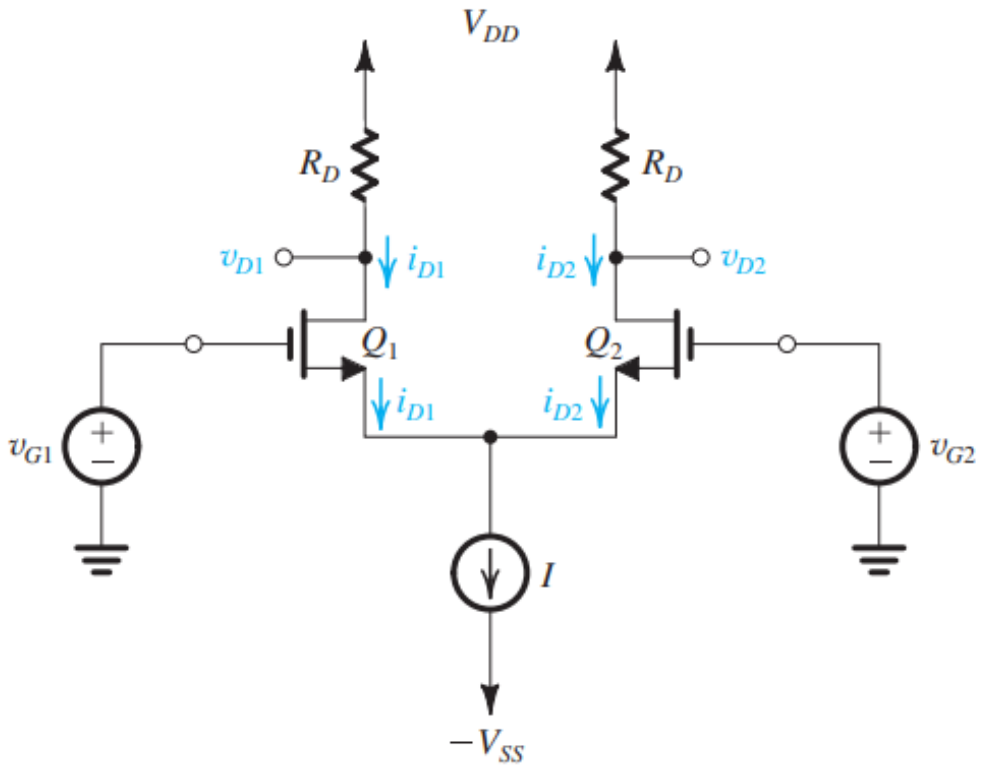

Figure 1.3: Differential Amplifier - Sedra and Smith

1.2.3 Gain

The purpose of an amplifier, bluntly stated, is to amplify the input signal. A quantification of how well this specific action is performed is known as the gain of the amplifier. Gain is a measure of the difference between power at the amplifier output and the input power, most commonly expressed as a ratio of output to input. Amplifiers will generally have at least two DC power supplies, positive and negative, also known as the "rails". This external DC power is applied to the input signal to produce a gain in power at the output.

In a single-ended amplifier, the overall gain is output over input. In a differential amplifier there are two inputs as well as two outputs. In this case, the output voltage is the difference between the two output ports, but the gain function remains the same,

output over input. Gain is of utmost importance when analyzing amplifiers in the frequency domain. As this thesis will focus on the time domain only, gain will not be measured or observed.

1.2.4 Beta

In bipolar junction transistors, the beta parameter denotes the current gain of a specific transistor. While MOSFETs are referred to as voltage-controlled devices, BJTs are current-controlled or current-driven. The current at the output (at the collector in this case) is a function of the current entering the base of the transistor. The current at the collector can be generally and quite accurately arrived at by multiplying the base current by the current gain, beta. This approximation is given below.

$$I_C = \beta \cdot I_B$$

1.3 Eye Diagram

Ideally, a digital clock signal fluctuates perfectly and instantaneously between “0” and “1”. In reality, however, a signal takes discrete amounts of time to rise to “1” and fall back to “0”. In the case of a differential, digital clock signal, one of the most descriptive tools to measure and compare minute variations in performance is the eye diagram. As frequency increases into the gigahertz range, it is more important than ever to identify effects of various system imperfections on signal integrity. An eye diagram essentially overlays a histogram of the “011”, “001”, “110”, and “100” bit patterns in one three-bit space. Figure 1.3 below shows an example of a generic eye diagram with common measurement criteria.

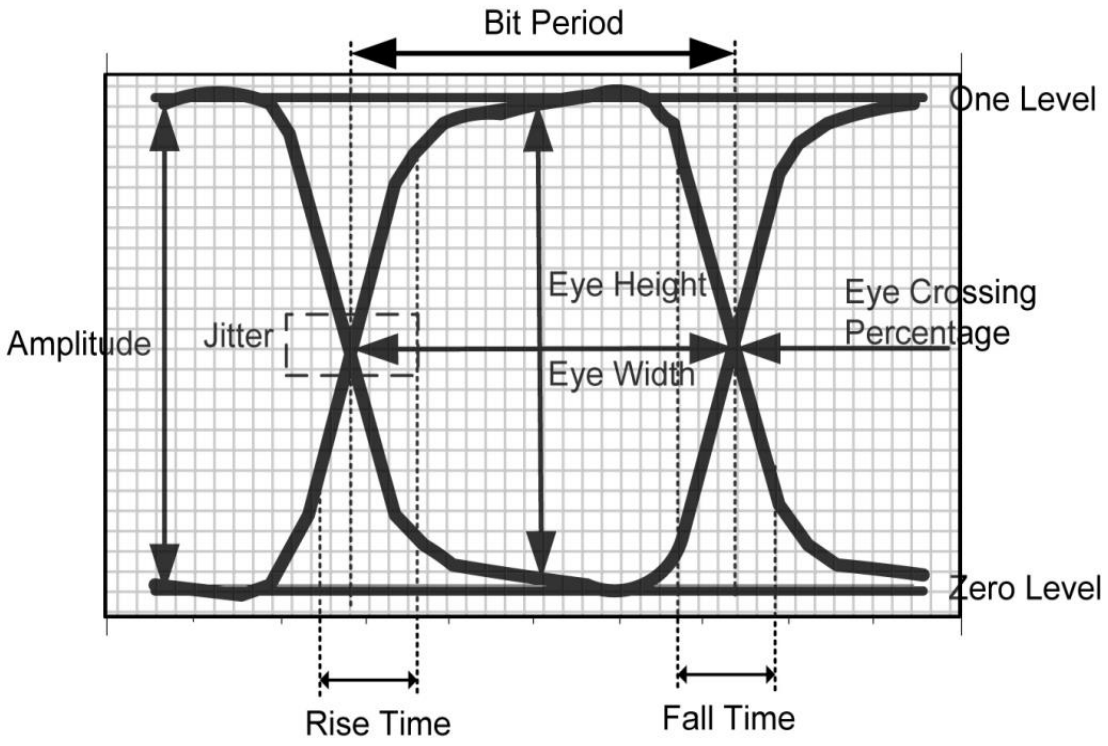

Figure 1.4: Eye Diagram Basics - OnSemi

1.3.1 Eye Height

The “1” and “0” levels are also known as high and low voltage levels, respectively. There is a small difference between eye amplitude and eye height, but both are essentially a difference between the 1 and 0 voltage levels, with eye height representing the difference between the lowest 1 voltage and the highest 0 voltage level. For the purpose of this thesis and as a result of limitations within the Advanced Design System software, this thesis will be focusing on eye height measurements and omitting eye amplitude.

1.3.2 Signal-to-Noise Ratio and Noise Margin

In real-world electrical signals, various sources of noise can cause significant problems with signal fidelity. The scope of this thesis will not, however, include real-world noise considerations. It will instead focus on noise margin and signal-to-noise ratio

as measured in the eye diagram. In an eye diagram measurement, the “high” or “1” voltage level can actually vary from bit to bit. The same is true of the “low” or “0” voltage level. This non-ideal variation leads to noise in the signal and closing of the eye, resulting in more difficult bit differentiation and increased errors. As measured, this phenomenon is known as signal-to-noise ratio, an indication of how well the signal can be identified through the noise. A signal-to-noise ratio of 1, or 1:1, describes half signal and half noise. An SNR of 10 describes a situation with ten times as much signal as noise A higher signal-to-noise ratio, or SNR, is desired.

Noise margin is similar to the signal-to-noise ratio, but more specific. The noise margin of a system gives a limit of how much noise can be added to a signal while the signal still maintains fidelity - is still able to properly differentiate 0s and 1s. Definitions and derivations for the high and low noise margins as a function of the high and low input/output voltages are given below, along with a diagram showing this relationship more clearly in figure 1.4.

$N_{ML} = V_{IL} - V_{OL}$

$N_{MH} = V_{IH} - V_{OH}$

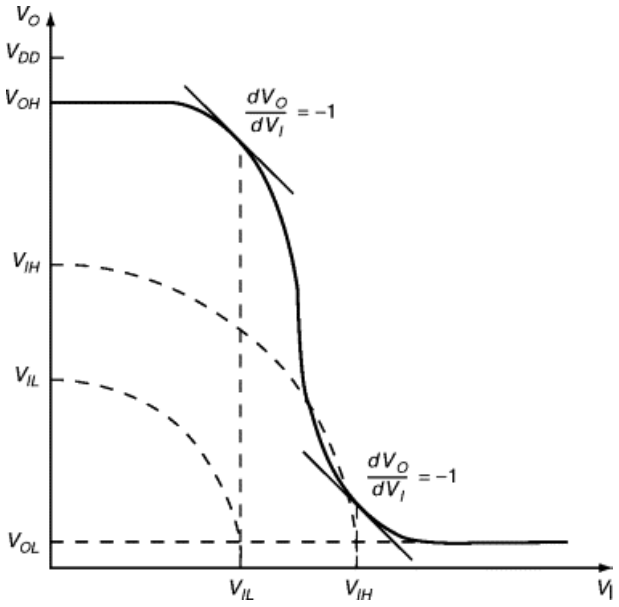

Figure 1.5: Noise Margin Voltage Levels – McShane and Shenai

1.3.3 Rise and Fall Time

The other parameter from the eye diagram of most significance to this thesis is the rise time. Fall time will also be measured, but these generally vary together. Rise time is the amount of time it takes for the signal to travel from the low voltage level to the high voltage level. On an ideal digital impulse signal, it's easy to consider the rise time as effectively zero. As mentioned previously, however, there is a finite amount of time that the signal spends increasing from low to high voltage level. The rise time is generally measured between 10% and 90% of the total voltage swing. As will be shown in this thesis, varying rise times in two parallel amplifiers can cause significant problems for timing and bit clarity. This can be most easily seen by use of an eye diagram measurement. Figure 1.5 below from MathWorks shows the rise time measurement on an eye diagram at the 10% and 90% voltage levels.

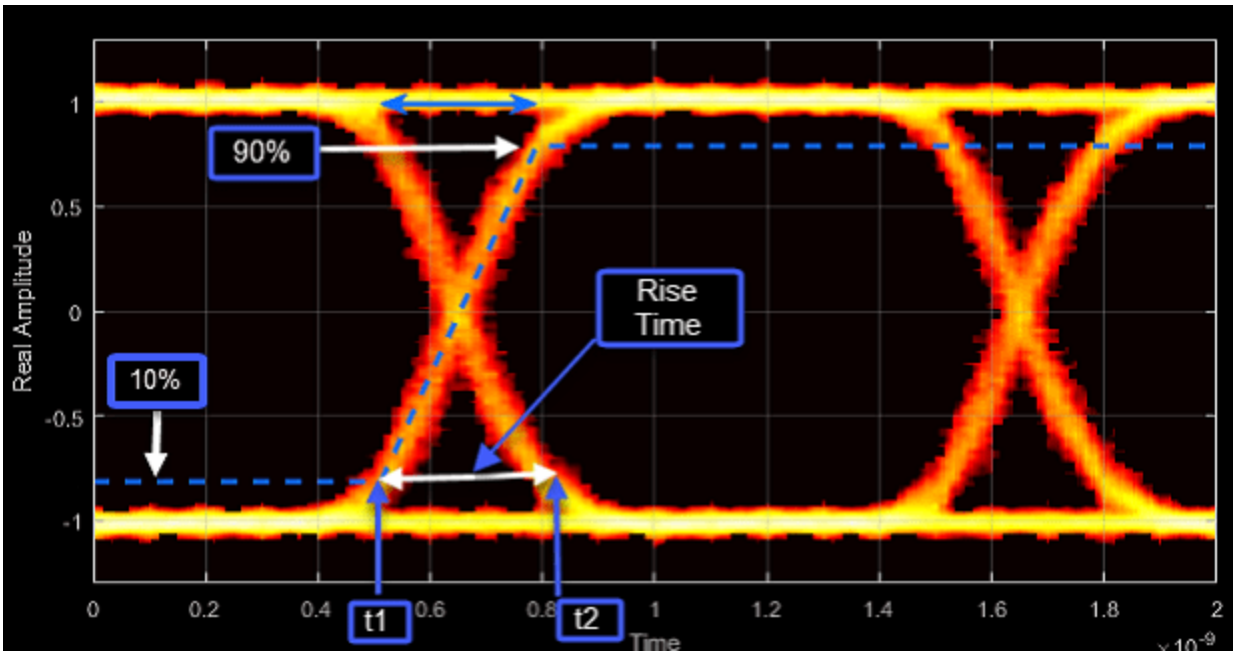

Figure 1.6: Eye Diagram Rise Time - MathWorks

1.4 Instrumentation Amplifier

There is currently one application of amplifiers regularly in use that is similar to the parallel configuration that will be presented in this thesis. The instrumentation amplifier generally employs three separate operational amplifiers; two operational amplifiers buffering the inputs and one output amplifier. A basic schematic from All About Circuits is shown in Figure 1.7 below.

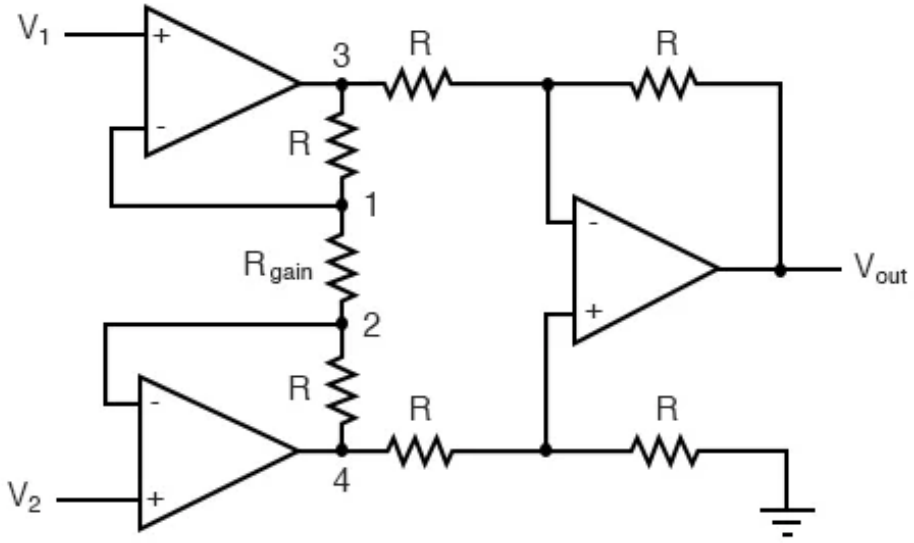

Figure 1.7: Instrumentation Amplifier - All About Circuits

In this case, it's not hard to see that the two input buffer amplifiers would need to be matched to some extent for proper operation. In an instrumentation amplifier, the gain of the entire amplifier circuit can be adjusted by changing only a single resistor value, R_{gain} in this case (All About Circuits, 2022). This circuit layout, however, is not primarily designed for high frequency or for digital signals. It is also a very complicated and cumbersome design. While it gives good gain control, the instrumentation amplifier is actually a very low gain device.

For the sake of simplicity and proof of concept, the remainder of this thesis will focus on single transistor amplifiers operating at a moderate frequency, in the single Gigahertz range,

CHAPTER 2 LITERATURE REVIEW

2.1 Introduction

There is a somewhat surprising gap in current literature regarding this specific parallel amplifier configuration. There is even less work done to investigate parallel amplifier mismatch in the time domain for digital signals. It is prudent, however, to first explore various sources of mismatch that can exist in the field of semiconductor electronics.

2.2 Process and Random Variations

As is the case with any real-world electronics application, integrated circuit fabrication is subject to random variations. Whether or not performance issues are caused, every semiconductor device on a single wafer will differ in some way. As integrated circuit components decrease further in size, however, smaller changes in the fabrication process and minute variations on a single wafer can have an increasingly significant effect on device performance. With increasing frequency demands, modern semiconductor devices must be as small as possible. These smaller gaps between components and more complicated fabrication challenges result in two sides of the same coin; the probability of seeing random process variations and defects increases with frequency, while the increasingly small semiconductor devices become even more susceptible and sensitive to those variations and defects.

2.2.1 Random Dopant Fluctuation

One of the most noteworthy variations that can occur during the MOSFET fabrication process is random dopant fluctuation. In the impurity doping process, the average number of dopant atoms in the channel region of a MOSFET can easily be less

than one thousand but can also vary from device to device. For this reason, as frequency increases and device size decreases, the fluctuations of dopant atom concentration in the channels have an increasing effect on variations in device performance (Marshall, 2009). Particularly at high frequencies, performance issues are caused not only by a fluctuation in the total number of impurities, known as average doping density, but also by variations in the "random distribution of impurities in the channel region", the specific locations of the impurities (Li & Hwang, 2008).

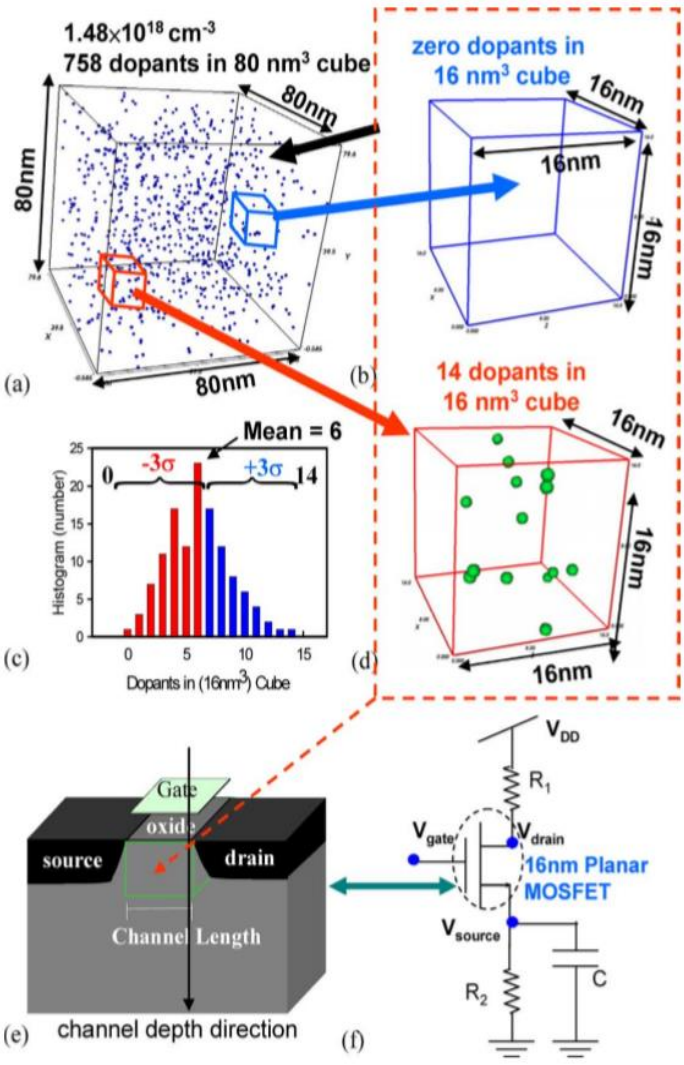

Figure 2.1: Random Dopant Fluctuations - Li and Hwang

Figure 2.1 above, from the Li and Hwang paper, gives a much further visual explanation of how dopant density can vary in (a) through (d), as well as a clear picture of the channel being discussed in (e) and (f). Another study found that "the nonuniform distribution of the dopant atoms…is a major contributor to the threshold voltage mismatch" (Lakshmikumar, Hadaway, & Copeland, 1986). It has been shown that the most notable performance issue caused by random dopant fluctuations is threshold voltage. Finally, this doping variation can also have a measurable effect on resistance and capacitance values at the semiconductor IC level.

2.2.2 Edge Roughness

Another key process variation that can result in mismatch performance issues is edge roughness. In this situation, nonuniformities in the photoresist and variations in the doping between the source and drain cause a variation or "roughness" in the edge that can affect the length and width of the gate (Marshall, 2009). One study also found that a prominent cause of mismatch performance issues is roughness on the edge of the polysilicon. Both the photolithography and etching processes in IC fabrication are vulnerable to random variations that can "induce effective polysilicon length variations" (Difrenza, et al., 2002). This same study claims that these length variations "can cause changes in the threshold voltage from transistor to transistor", a theory that will be tested experimentally in a following section. These variations as a result of edge roughness were also corroborated by Shyh-Chyi Wong et. All (Wong, Pan, & Ma, 1997). An additional paper by Asen Asenov et. All set up various simulations to model and measure the implications and effects of this edge roughness, and their findings match up with those of

the previous papers (Asenov, Brown, Davies, Kaya, & Slavcheva, 2003). Similar to random dopant fluctuations, edge roughness issues can result in variations in resistance and capacitance values.

2.2.3 Work-Function Fluctuation

A study by Han, Li, and Hwang investigated the influence of multiple parametric changes, including random dopant fluctuation. One parameter studied in this experiment that is not common in other studies is work-function fluctuation, referred to as WKF. This random variation in MOSFET fabrication is a result of metal being used as the gate material, and it has been known to cause further fluctuations in threshold voltage. This study found, however, that the effect of WKF on threshold voltage fluctuations is significantly less than that of the random dopant fluctuations mentioned in a previous section. In addition, WKF seems to have a negligible effect on gate capacitance and cutoff frequency, and the same is true about its effect on circuit gain and power at higher frequencies (Han, Li, & Hwang, 2010). The random dopant fluctuations have been found to have a much more significant impact than WKF, so it will not be considered as relevant to this thesis.

2.2.4 High-Frequency Effects

In semiconductors and electronics in general, it has been proven that increases in frequency result in many new design challenges. A future section will go into the effects of mismatch at high frequencies. In addition to mismatch performance issues, however, higher frequencies also introduce unique fabrication complications and imperfections. For higher frequency semiconductor devices, the overall device dimensions and scales are drastically reduced. As this size decreases the random variations in fabrications have

a more detrimental effect. One study found that “with device scaling, various randomness effects resulting from the random nature of manufacturing process, such as ion implantation, diffusion, and thermal annealing, have induced significant fluctuations of electrical characteristics in nanometer scale (nanoscale) MOSFETs” (Li & Hwang, 2008). Another study determined that, at high frequencies, random dopant fluctuations and process variation effect have a relevant impact on circuit gain and power efficiency (Han, Li, & Hwang, 2010).

2.3 Mismatch

The previous section outlined the more common process variations seen in semiconductor devices. Beyond this, however, these imperfections and variations can result in even more significant differences between individual devices on the same wafer, let alone on different wafers. These semiconductor devices are designed to be identical and would be in an ideal case. Due to the previously mentioned minute imperfections and variations, however, two devices with the same design will have slight random variations in physical characteristics and performance, even when fabricated on the same wafer. This problem of variation is known as mismatch, and it has caused decreases in device yield and performance throughout the history of semiconductor technology. Patrick Drennan and Colin McAndrew claimed that in history, many in the field of semiconductor devices have made the mistake of treating mismatch in ICs as more of an art than a science, designing and simulating on the basis of previous experience and guesswork rather than proven characterized models of mismatch (Drennan & McAndrew, 2003).

2.3.1 Mismatch on a Single Integrated Circuit

There is substantial research investigating mismatch between two devices on a single integrated circuit. One example of this is multiple current mirrors on a single amplifier chip, which can be seen in Figure 2.2 below.

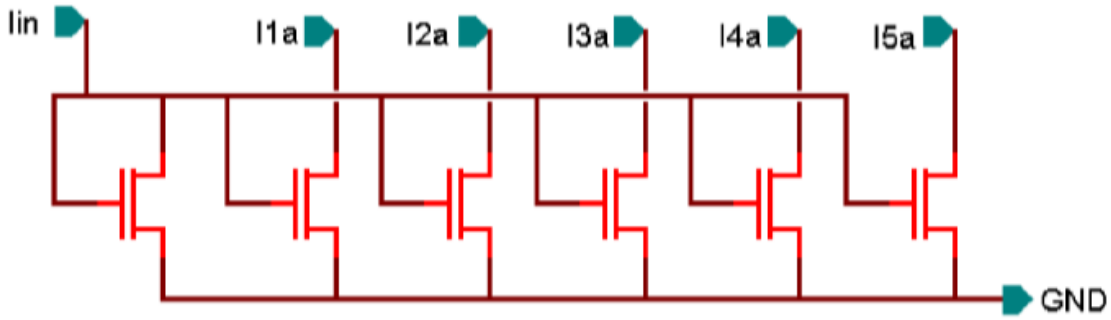

Figure 2.2: Basic Current Mirror Structure - Marshall

In his 2009 book titled *Mismatch and Noise in Modern IC Processes*, Marshall recounts the idea that the successful operation of a current mirror relies on a matching between the output current transistor and the input current transistor in order to properly duplicate the current. Even when fabricated on the same wafer for a single IC, variations in these two transistors can very easily result in unmatched current at the input and output, potentially compromising the basic performance of the current mirror (Marshall, 2009). This problem is only amplified in more and more complex integrated circuits, with every extra transistor introducing another opportunity for mismatch. In addition, it has been proven that the mismatch problem in MOSFETs is intensified as the signal swing available decreases with device dimensions (Pelgrom, Duinmaijer, & Welbers, 1989). Patrick Drennan and Colin McAndrew investigated mismatch in current mirrors as well, finding that mismatch is much more affected by changes in transistor length than width (Drennan & McAndrew, 2003).

2.3.2 Mismatch Caused by Random Dopant Fluctuations

As discussed previously, variations in the concentration and location of impurities in MOSFET channels can cause significant performance issues at the device level. One study experimentally showed that, as doping concentration within the channel increases, the threshold voltage also increases. In addition, there is also a decrease in transistor current (in the on state) and a corresponding increase in output voltage and output resistance as the number of dopants increases (Li & Hwang, 2008). These are all quantities that will be measured and verified in the following experimental sections. As semiconductor devices are all subject to random variations in dopant density during fabrication and it has been shown that increases in dopant concentrations result in measurable changes in threshold voltage, transistor current, output voltage, and output resistance, it follows that random dopant fluctuations will be a significant cause of mismatch in a MOSFET amplifier, especially as frequency increases. A study by Gabriele Tocci in 2010 investigated random dopant fluctuations more closely. Figure 2.3 below shows actual dopant placement in spatial positions, while Figure 2.4 below gives a 3-dimensional cross-section of the dopant distribution.

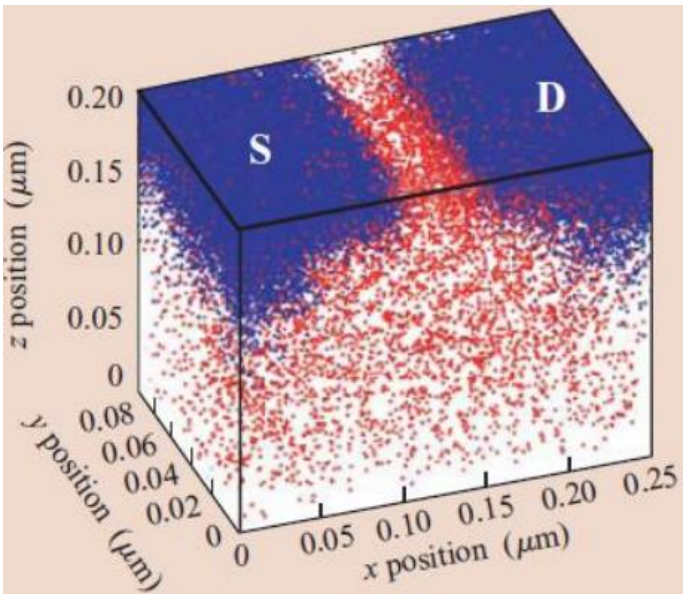

Figure 2.3: Dopant Placement - Tocci

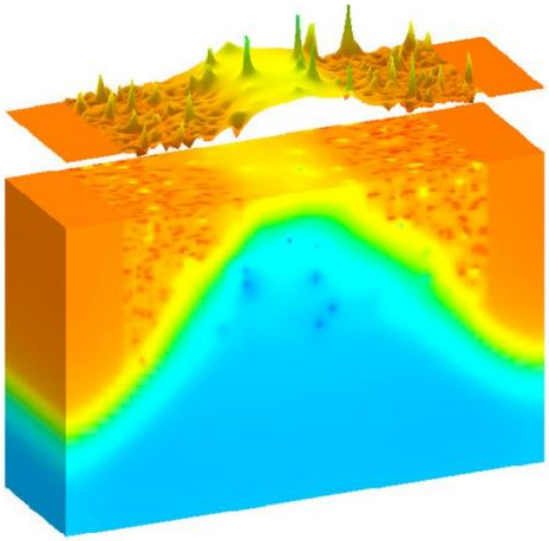

Figure 2.4: Doping Cross-Section - Tocci

This same investigation by Gabriele Tocci plotted the distribution of threshold voltages for devices with varying random dopant fluctuations, clearly showing a fairly significant variation (Tocci, 2010). This distribution is shown below in Figure 2.5.

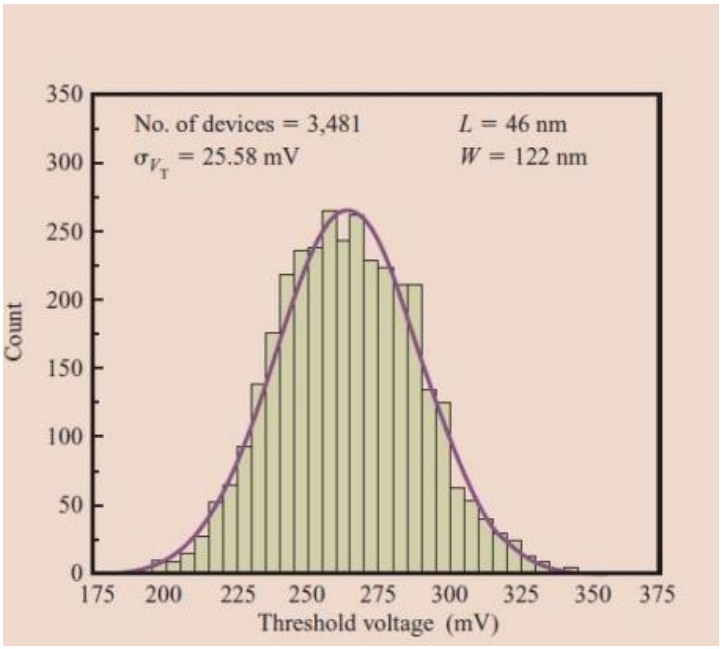

Figure 2.5: Threshold Voltage Distribution - Tocci

2.3.3 Mismatch Caused by Edge Roughness

The previous section showed that much research has been done to prove that problems with "edge roughness" can result in significant variations in width and length of the device gate. S. J. Lovett et. All performed extensive experiments to characterize the dependence between device geometry and mismatch, with the result that devices with small W/L ratios have generally much better matching properties than those with larger W/L ratios (Lovett, Clancy, Welten, Mathewson, & Mason, 1996). As seen in the previous section, roughness on the edge can cause significant variations in width and length of devices, so this further outlines the effect of varying edge roughness on device mismatch. These changes can also effect resistance values on devices within a single wafer.

2.3.4 Mismatch at High Frequencies

In modern semiconductor devices and electronics in general, it has been continuously proven that increases in frequency can result in significant increases in performance sensitivity to minute physical variations and circuit and device mismatch. At higher frequencies, capacitances must be significantly smaller. Thus, overall transistor device dimensions are drastically reduced as frequency increases. Smaller devices then, as shown previously, are far more sensitive to process variations like random dopant fluctuations and edge roughness variations. In addition, these smaller devices operating at faster and faster speeds are subject to significant mismatch issues. Separate elements of a traditional radio frequency (RF) circuit must be matched at as close to 50 ohms as possible. When this match is less than perfect, there is some amount of signal and power loss that is directly proportional to signal frequency.

2.3.5 Mismatch Between ICs on Separate Wafers

In broad electronics, it is generally rare that two ICs being used at one time were actually fabricated on the same wafer. We previously saw that devices on a single wafer are subject to variations that can result in performance differences between the devices on that wafer. It follows that the variations between two devices from separate wafers will be even more pronounced, resulting in even more significant performance differences between these two separate devices. One study that actually briefly looked into mismatch differences between single devices and multiples devices in parallel, such as a differential amplifier, found that the mismatch is expected to increase as the number of devices connected in parallel at the reference side increases, but that this may not be the case when looking at multiple devices connected at the output (Drennan & McAndrew, 2003).

Taking this yet another step further, even more mismatch is expected in an application that requires two random “equivalent” devices operating in a way that relies on their similarities for ideal performance. This mismatch is expected to increase at higher frequencies, specifically in the gigahertz range. The next section will attempt to prove this theory by first designing a common-base BJT amplifier, placing two in parallel, and simulating the parallel configuration in Advanced Design System. The output will be measured using the eye diagram utility in ADS.

CHAPTER 3 METHOD

3.1 Research Question

It has been proven that there is measurable variation between separate integrated circuits on a single semiconductor wafer, and that this variation can result in performance mismatch between the individual ICs. This will likely be seen when measuring characteristics of two separate amplifier ICs that are "identical" on paper. Taking this a step further, however, it is expected that two individual amplifiers connected in parallel to amplify both sides of a differential line will see increased performance mismatch as a result of the process variation and fabrication differences between the two ICs. This effect is expected to increase with frequency.

The following section will outline two experiments related to this problem. The first will be a theoretical derivation of expected parameter drift as a result of mismatch in a BJT common-base amplifier circuit. The second will be design and simulation of this amplifier in Spice and Advanced Design System software to hopefully prove and verify the accuracy of the theoretical predictions and models.

3.2 Software Tools

This thesis employed the use of two primary design and simulation tools: LTspice for proof-of-concept and Advanced Design System for advanced simulation and eye diagram utility. Both programs offer the ability to import and utilize real-world transistor models for far more simulation accuracy.

3.2.1 LTspice

SPICE, which stands for Simulation Program with Integrated Circuit Emphasis, is an open-source circuit design and analysis program that is quite widely used. Spice

software is common in both educational and professional environments primarily for its simplicity and versatility. The version of spice used in this thesis is LTspice (version XVII), a spice program by Analog Devices. The general interface of LTspice is shown in Figure 3.1 below. LTspice is used in this experiment to first create a proof-of-concept amplifier design before venturing into the complexities of ADS.

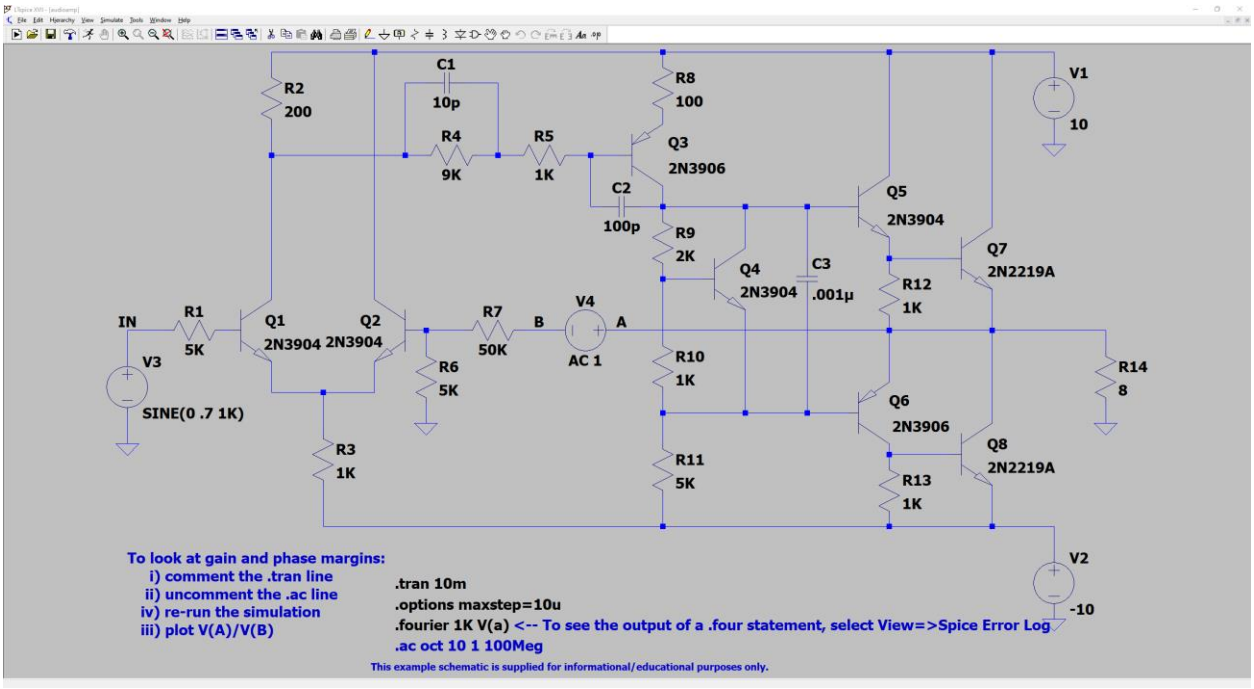

Figure 3.1: LTspice Interface

3.2.2 PathWave Advanced Design System

PathWave Advanced Design System, also known as ADS, is a complex and powerful electrical design and simulation program designed and owned by Keysight Technologies. While including all of the functionality a spice program offers, ADS provides a host of more advanced simulation utilities. This ranges from better high-frequency simulation accuracy to three-dimensional electromagnetic modeling, in addition to the eye diagram probe and utility used extensively in this experiment. An

example schematic is shown in Figure 3.2 below with the standard ADS software interface.

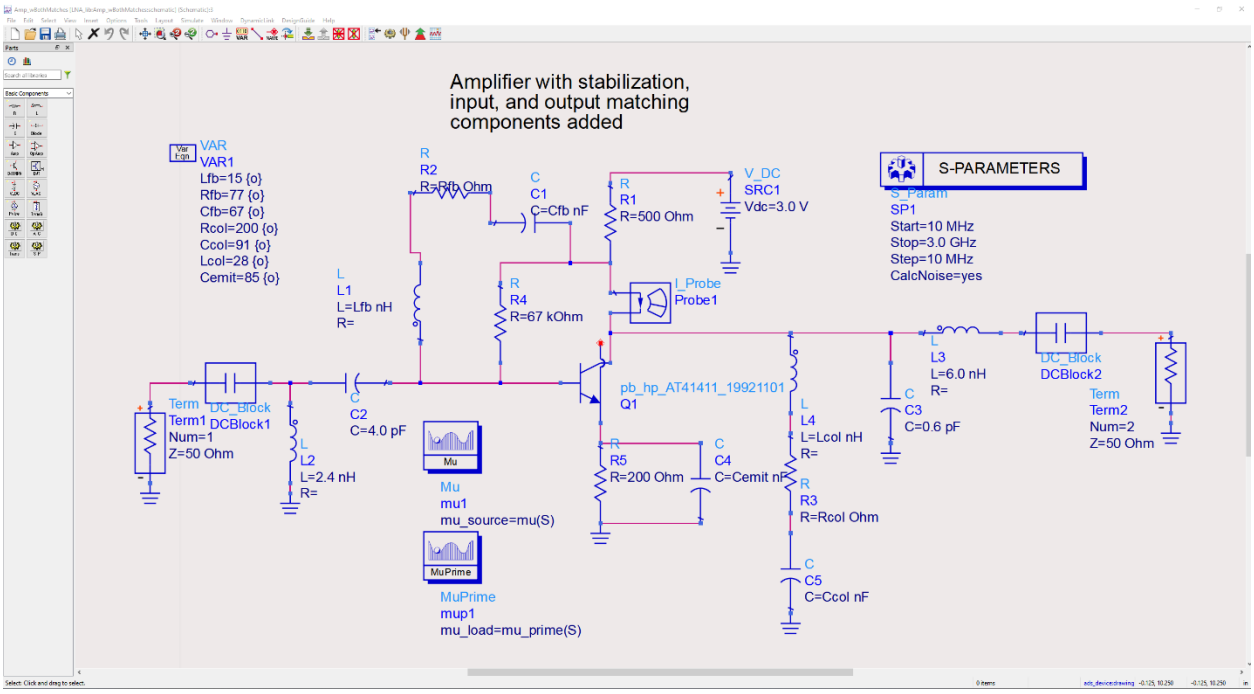

Figure 3.2: Advanced Design System Interface

3.3 Measurement Criteria

This section will outline and describe the criteria that will be measured on each amplifier or pair of amplifiers to compare results and, hopefully, measure performance mismatch.

3.3.1 Eye Height and Width

The primary measurement in this experiment is a differential eye diagram at the output. An eye diagram overlays the 011-, 001-, 100-, and 110-bit patterns in one window with specific focus on the empty space, or eye, in the center. Figure 3.3 below shows basic steps in the creation of an eye diagram.

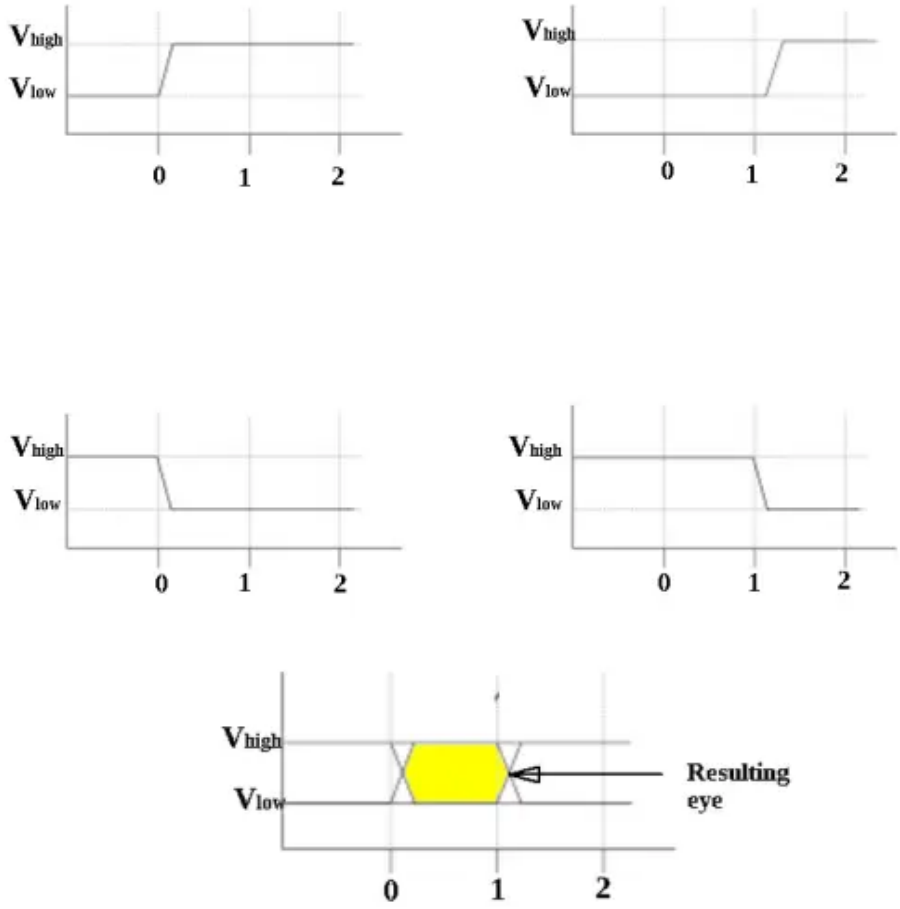

Figure 3.3: Eye Diagram Creation - Test and Measurement Tips

The eye height in an eye diagram is generally measured as a difference between the measured high ("1") and low ("0") voltage levels, with the eye width a measurement between the eye crossing points.

3.3.2 Rise Time and Fall Time

On an ideal digital signal, the voltage could change from zero to one instantaneously. In a real signal, however, the rise time is the amount of time it actually takes for the signal to swing up to the high voltage position. The fall time is the same

quantity measured for the signal swinging back down to low or zero voltage. In practice, the rise time is generally measured between the 10% and 90% voltage levels.

3.3.3 Jitter

A purely theoretical ideal electrical signal is perfectly periodic. A real-world electrical signal will vary slightly in time or amplitude, resulting in what is known as jitter. The first type of jitter, random, is unpredictable and generally caused by thermal noise. The second, deterministic jitter, is repeatable and generally predictable, in addition to being bounded. The eye diagram is a very popular method of measuring jitter. In an eye diagram, jitter is seen at the widening of bit crossing points.

3.4 Procedures

This section will outline the procedures and methods used to measure the various characteristics of the individual op amp ICs.

3.4.1 Proof of Concept Spice Simulation

Before entering into the complexity and extra functionality of the ADS software, the basic single amplifier layout was designed, built, and simulated in LTspice software. The schematic is shown below in Figure 3.4.

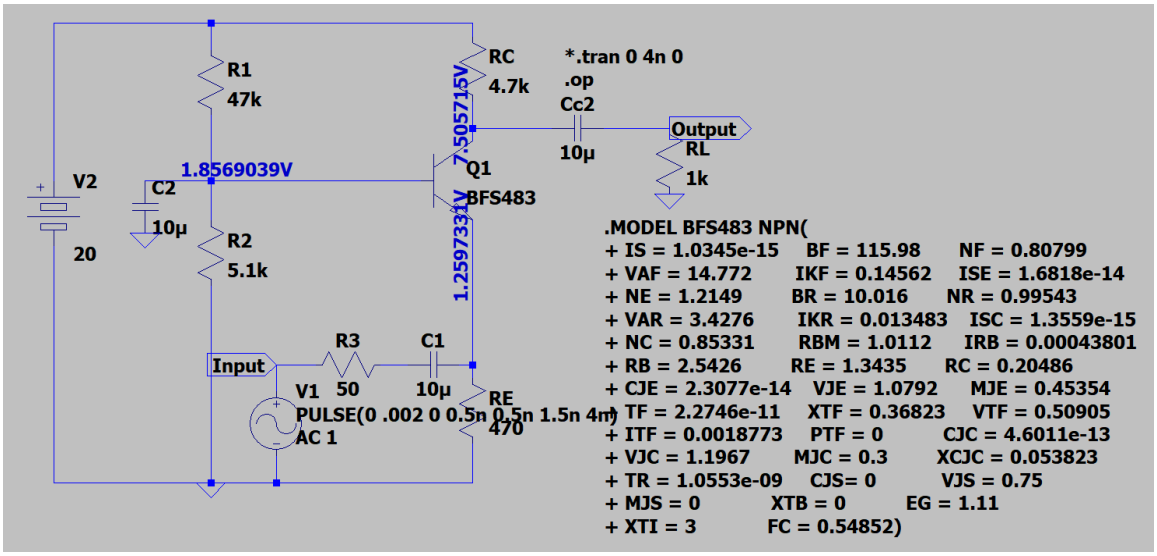

Figure 3.4: Spice Schematic

This initial simulation was used to test basic DC biasing and input pulse functionality on the individual amplifier. A real-world model for the BJT (BFS483) was included in the LTspice simulation and copied over into the ADS software. The digital input pulse simulation for proof-of-concept is given in Figure 3.5 below.

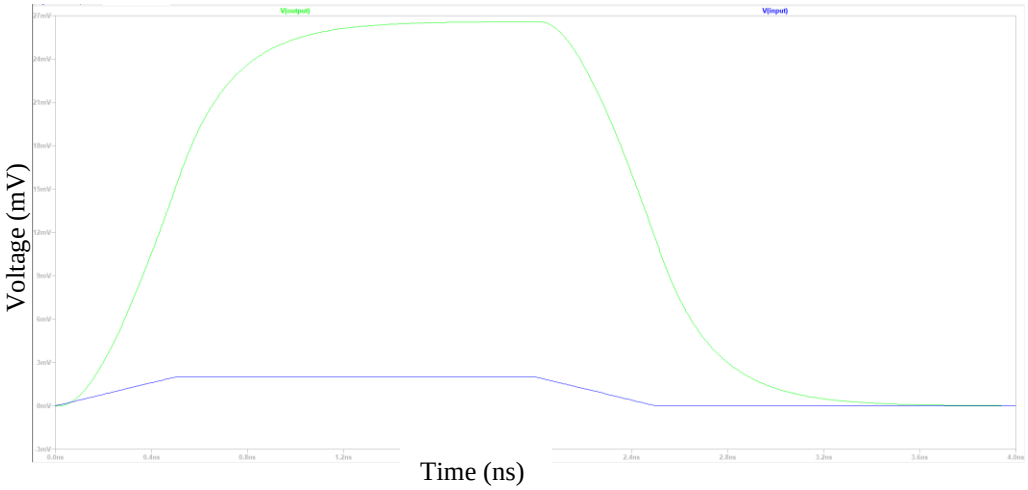

Figure 3.5: Spice Design Simulation

Following sections will show that the amplifier design went through multiple iterations, changes, and improvements in the ADS software when compared with this original LTspice layout.

3.4.2 ADS Design

The design shown previously from LTspice was built in the Keysight Advanced Design System software and then copied and modified. The basic single amplifier layout was copied in ADS to create the desired dual parallel amplifier, with inverse digital pulse signals at the two inputs. The BJT model had to be imported manually into an ADS transistor model. The ADS design is shown below in Figure 3.6.

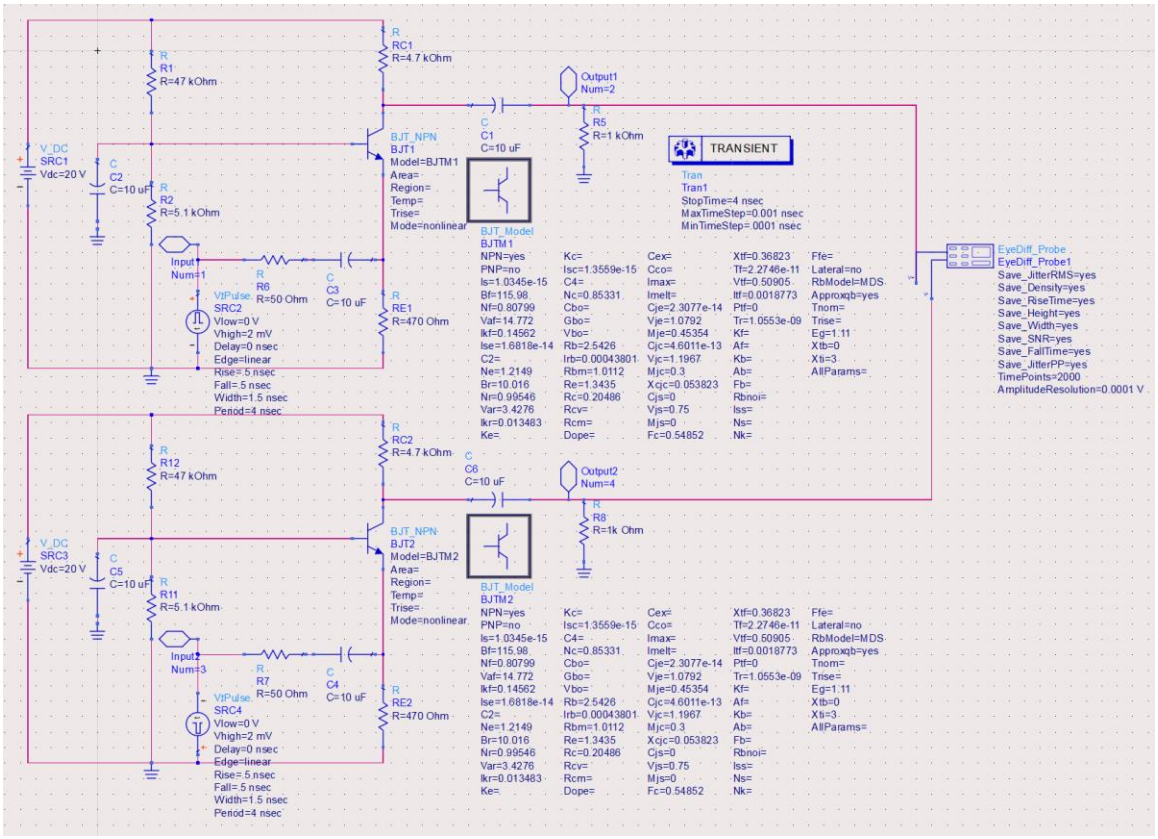

Figure 3.6: ADS Schematic

3.4.3 Design Considerations

Throughout the design and simulation process many choices had to be made for the sake of specific performance needs. For the BJT, a common-base amplifier was chosen in consideration of 50-ohm impedance matching.

3.4.4 Specifications

The inspiration for this thesis came from a need for parallel amplifiers on a differential line at quite high frequencies reaching double-digit gigahertz ranges. In this thesis, however, this need is generalized and simulated at a much lower frequency. The specification for USB 2.0 has a signal rate of 480 Mbit/s. As it is a differential signal, the actual signal frequency is half this, at 240 MHz. Using this specification as inspiration, this thesis employs an input signal frequency of 250 MHz. Also taken loosely from the USB 2.0 specification is the logical high voltage level of 2mV.

3.5 Derivations and Calculations

In addition to setting up simulations and experiments, it is first necessary to investigate and outline the mathematical relationships presented and compared in this thesis. Starting from the end, the eye diagram will be the final measure of performance differences and changes. The eye height shows the most significant variations as a result of various operational amplifier parameter differences. Unfortunately, eye height specifically is not easy to determine or define mathematically on its own. It is therefore prudent to focus on the rise time of the signal in place of the eye height, as the signal's rising (and falling) edge primarily makes up the generation and structure of the eye diagram and the eye height measurement. An approximation relating rise time and bandwidth of electrical systems – amplifiers in this case – has been derived and used countless times in academia. This equation is shown below. In this case, rise time is calculated at the ten and ninety percent voltage levels. This relationship is derived from the RC time constant equation and the transient signal voltage as a function of time equation (Bogatin, 2018).

$$t_r \cong \frac{0.35}{BW_{3dB}}$$

It is important to note that this is only a rough approximation and can certainly vary from case to case, but it will serve well to estimate approximate effects on rise time from various parameters and to verify the validity of the simulation.

3.5.2 Spice Calculations

The spice model shown above was also used to calculate some important parameters needed in future theoretical derivations. The specific change for this step was commenting out the transient simulation to run a simple operating point simulation. In LTspice, after running an operating point simulation, certain internal parameters of the BJT are measured/calculated and output the log file. A portion of this log file is given below in Figure 3.7.

```
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- Bipolar Transistors ---
Name:       q1
Model:    bfs483
Ib:       2.19e-05
Ic:       2.66e-03
Vbe:      5.97e-01
Vbc:     -5.65e+00
Vce:      6.25e+00
BetaDC:   1.21e+02
Gm:       1.25e-01
Rpi:      9.94e+02
Rx:       2.40e+00
Ro:       6.72e+03
Cbe:      2.87e-12
Cbc:      1.47e-14
Cjs:      0.00e+00
BetaAC:   1.24e+02
Cbx:      2.58e-13
Ft:       6.31e+09
```

Figure 3.7: LTspice Log File for Internal Capacitances

The parameters calculated and measured here that are of importance to this experiment are r_π, C_{be}, and C_{bc}. These will be used in generating a modeled equation for the time constant τ. For the sake of clarity these values are given below.

r_π = 9.94e2 Ω = 994 Ω

C_{BE} = 2.87e-12 F = 2.87 pF

C_{BC} = 1.47e-14 F = 14.7 fF

3.5.3 Small-Signal Model

A small signal model was created for the single BJT common-base amplifier circuit design in order to model and predict circuit performance at high frequencies. This rough model is shown below, with alterations for calculating open-circuit time-constants.

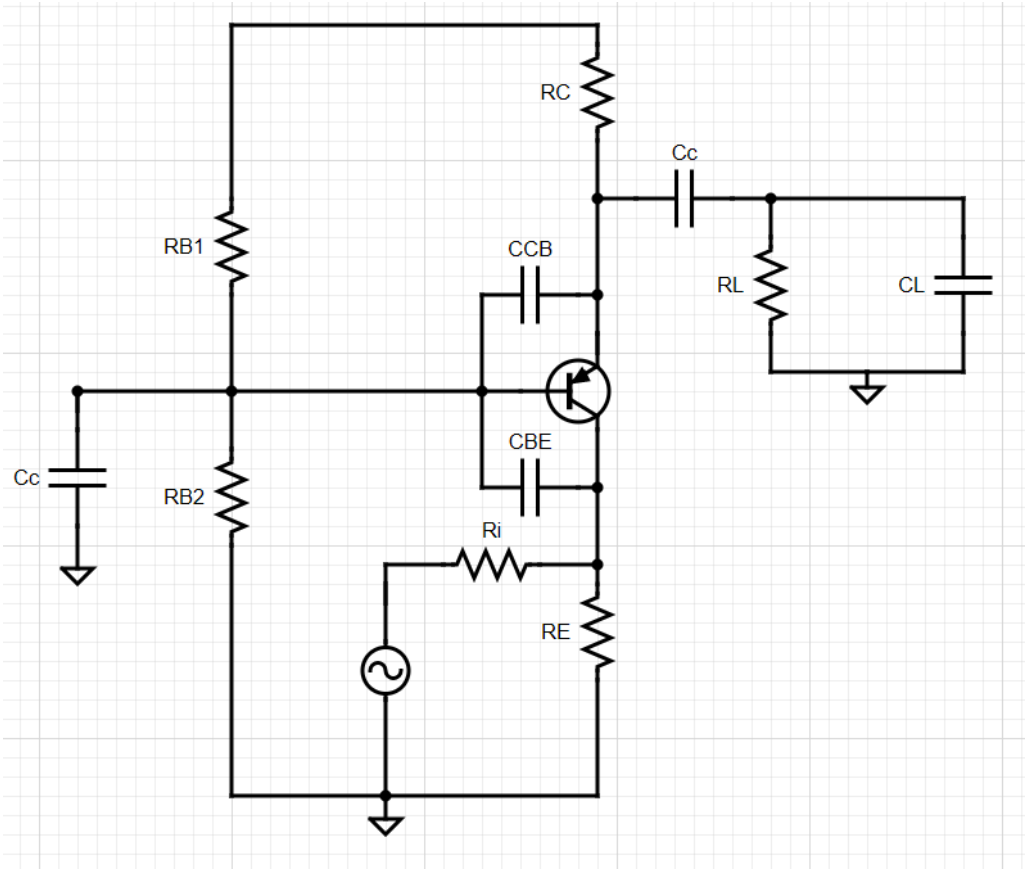

Figure 3.8: CB Amplifier Schematic

Figure 3.8 above shows a basic common-base BJT amplifier circuit design. This model includes internal capacitances C_{CB} and C_{BE}, which will be included in the following small-signal models.

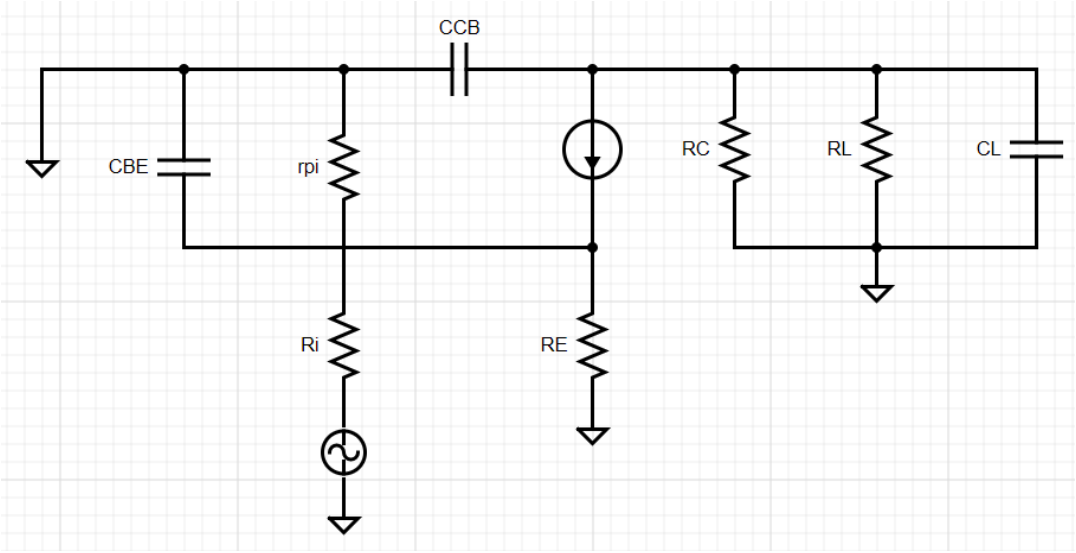

Figure 3.9: Small Signal Model

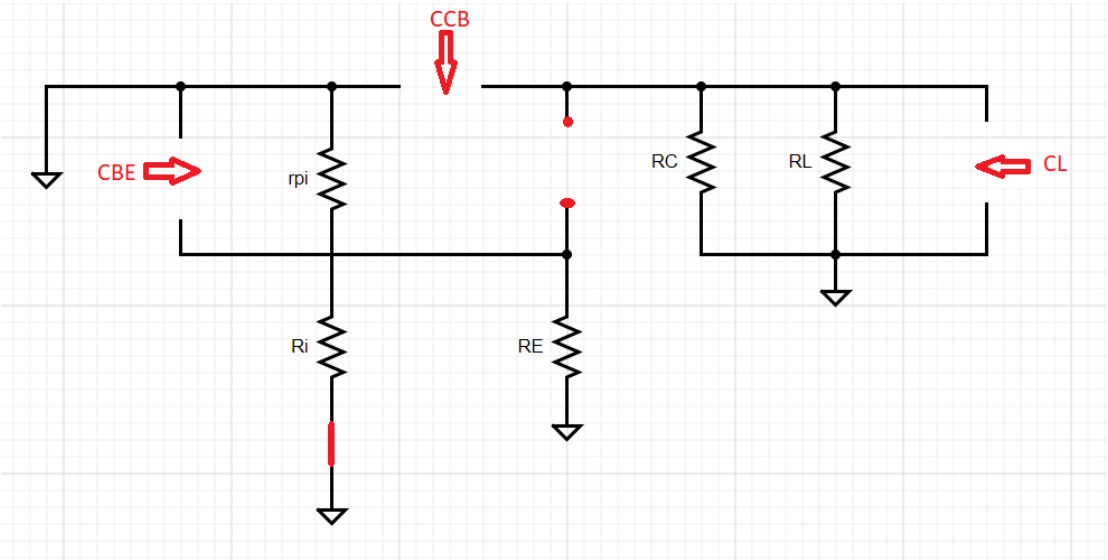

Figure 3.10: High Frequency Small Signal Model for Open-Circuit Time-Constants

Figure 3.9 shows a generic small-signal model of the CB amp circuit, with Figure 3.10 showing the final modification of the small-signal model to calculate open-circuit time constants. Here the dependent current source is opened at high frequencies and the voltage source is shorted.

3.5.4 Open-Circuit Time Constants

When working with complex circuit designs at high frequencies, calculating a single time constant for an amplifier circuit can be quite difficult. The primary challenge here is in calculating a single equivalent resistance and capacitance. There exists a method of working around this problem that involves setting all capacitances to zero (and shorting sources) and then calculating equivalent resistance as seen by each capacitance, one at a time. This method is known as calculating open-circuit time constants. After each individual equivalent resistance and time constant has been calculated, the sum of all individual time constants results in a very accurate approximation of a single time constant for the full circuit. Another large benefit of this method is that it separates individual poles and zeros of the circuit, making it fairly easy to identify a dominant pole and dominant time constant if one exists.

Using the method of open-circuit time constants and the small signal model with capacitances above, the following good approximation for the time constant of this single BJT amplifier circuit was derived:

$$\tau = (R_i // R_E // r_\pi)C_{BE} + (R_C // R_L)C_{CB} + (R_C // R_L)C_L$$

The internal capacitances and r_π values from the Spice circuit simulation above were plugged into this τ equation, along with 50 Ω for R_i and 1 kΩ for R_L, for the following result:

$$\tau = \frac{47.6R_E}{47.6+R_E}(2.87\times10^{-12}) + \frac{1000R_C}{1000+R_C}(14.7\times10^{-15}) + \frac{1000R_C}{1000+R_C}(1\times10^{-12})$$

Table 3.1 and table 3.2 below show rough sweeps of R_C and R_E and the resulting pieces of the time constant equation.

RC	RE	CBE	CCB	CL		**TCBE**	TCCB	TCL	T
4640	470	2.87E-12	1.47E-14	1.00E-14		**1.24E-10**	1.21E-11	8.23E-12	1.44E-10
4660	470	2.87E-12	1.47E-14	1.00E-14		**1.24E-10**	1.21E-11	8.23E-12	1.44E-10
4680	470	2.87E-12	1.47E-14	1.00E-14		**1.24E-10**	1.21E-11	8.24E-12	1.44E-10
4700	470	2.87E-12	1.47E-14	1.00E-14		**1.24E-10**	1.21E-11	8.25E-12	1.44E-10
4720	470	2.87E-12	1.47E-14	1.00E-14		**1.24E-10**	1.21E-11	8.25E-12	1.44E-10
4740	470	2.87E-12	1.47E-14	1.00E-14		**1.24E-10**	1.21E-11	8.26E-12	1.44E-10
4760	470	2.87E-12	1.47E-14	1.00E-14		**1.24E-10**	1.21E-11	8.26E-12	1.44E-10
4780	470	2.87E-12	1.47E-14	1.00E-14		**1.24E-10**	1.22E-11	8.27E-12	1.44E-10
4800	470	2.87E-12	1.47E-14	1.00E-14		**1.24E-10**	1.22E-11	8.28E-12	1.44E-10
4820	470	2.87E-12	1.47E-14	1.00E-14		**1.24E-10**	1.22E-11	8.28E-12	1.45E-10

Table 3.1: Time Constant Sweeps for R_C

RC	RE	CBE	CCB	CL		**TCBE**	TCCB	TCL	T
4700	410	2.87E-12	1.47E-14	1.00E-14		**1.22E-10**	1.21E-11	8.25E-12	1.43E-10
4700	430	2.87E-12	1.47E-14	1.00E-14		**1.23E-10**	1.21E-11	8.25E-12	1.43E-10
4700	450	2.87E-12	1.47E-14	1.00E-14		**1.24E-10**	1.21E-11	8.25E-12	1.44E-10
4700	470	2.87E-12	1.47E-14	1.00E-14		**1.24E-10**	1.21E-11	8.25E-12	1.44E-10
4700	490	2.87E-12	1.47E-14	1.00E-14		**1.25E-10**	1.21E-11	8.25E-12	1.45E-10
4700	510	2.87E-12	1.47E-14	1.00E-14		**1.25E-10**	1.21E-11	8.25E-12	1.45E-10
4700	530	2.87E-12	1.47E-14	1.00E-14		**1.25E-10**	1.21E-11	8.25E-12	1.46E-10
4700	550	2.87E-12	1.47E-14	1.00E-14		**1.26E-10**	1.21E-11	8.25E-12	1.46E-10
4700	570	2.87E-12	1.47E-14	1.00E-14		**1.26E-10**	1.21E-11	8.25E-12	1.46E-10
4700	590	2.87E-12	1.47E-14	1.00E-14		**1.26E-10**	1.21E-11	8.25E-12	1.47E-10

Table 3.2: Time Constant Sweeps for R_E

The C_{BE} and emitter resistance portion of this time constant is dominant, but not by much. This is shown in Table 3.1 with the time constant (T in this table) effectively remaining constant as R_C is swept. Table 3.2 shows more significant time constant dependence on R_E.

CHAPTER 4 RESULTS AND DISCUSSION

4.1 Introduction

It has been proven that there is measurable variation between separate integrated circuits on a single semiconductor wafer, and that this variation can result in performance mismatch between the individual ICs. This section outlines and presents the results of a circuit simulation experiment attempting to identify and model the effects of parallel amplifier mismatch as measured in an eye diagram.

4.2 Mismatch Characterization

It is first important to identify and clarify how mismatch will be isolated and characterized in the following experiments. The main parameter that will be used to track parameter mismatch will be a delta value. For the sake of clarity, this example will consider the collector resistance change. ΔR_C will be given as a percentage change value as derived below. Note that R_C is a temporary parameter used in the ΔR_C calculation as shown below.

$$\triangle R_C = \frac{|R_{C1} - R_{C2}|}{R_C}$$

$$R_C = \frac{R_{C1} + R_{C2}}{2}$$

4.3 ADS Simulation Parameter Sweeps

Figure 4.1 is the schematic for the circuit layout used in the following amplifier parameter sweeps, as well as the simulation window showing eye height and eye width measurements in Figure 4.2.

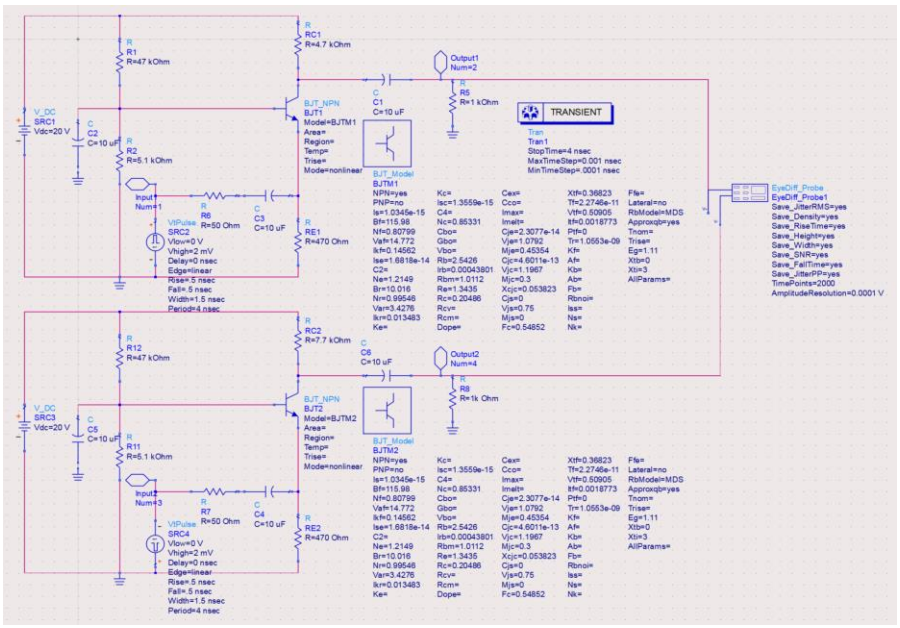

Figure 4.1: Final ADS Schematic for Eye Diagram Measurements

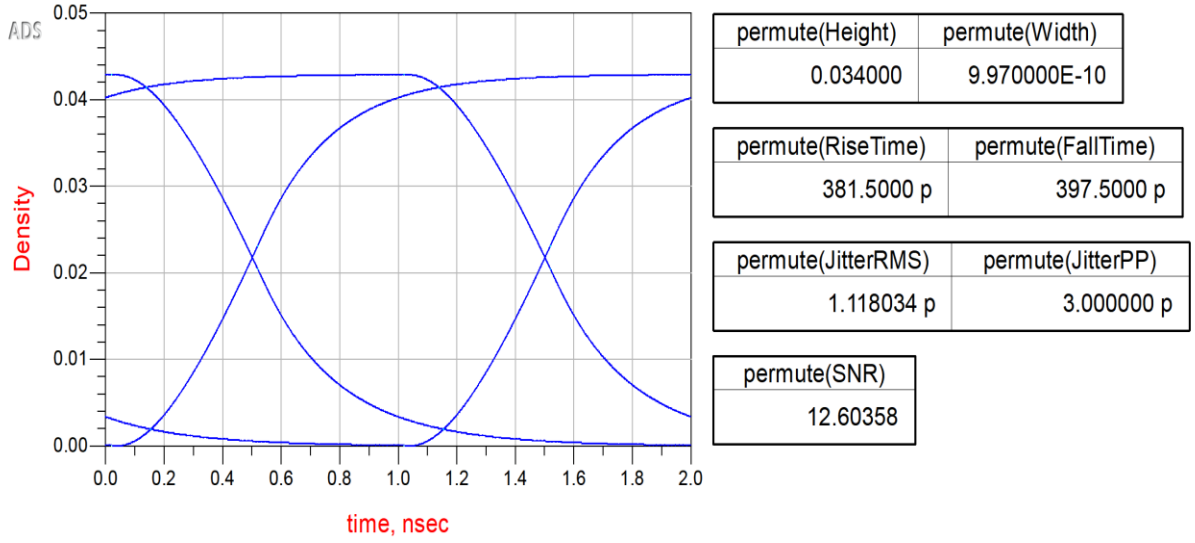

Figure 4.2: Final ADS Eye Diagram Simulation Window

The sweeps were carried out on a single variable at a time, both for mismatch between the two amplifiers and general dependance on matched parameters as a baseline. Eye width did not vary for any of the following sweeps, so it was omitted from the tables and plots.

4.3.1 Collector Resistance

The first parameter swept was the collector resistance on the second/bottom amplifier. The starting value for both, and the value at which the top amplifier was held, is 4.7 kOhms. This value came from a general optimization of the design for gain. The bottom collector resistance was swept from 4.7k to 7.3k with a 200-ohm step size. For each of these collector resistance pairs, a value of ΔR_C (Delta RC) is calculated and given as a percentage change value. Using the EyeDiff_Probe component/tool in ADS, the eye height and width, rise and fall times, jitter, and signal-to-noise ratio were all measured at each step. The results from this sweep are in Table 1 below.

RC1 (ohms)	RC2 (ohms)	RC	Delta RC	Delta RC (%)	Eye Height	Eye Width	Rise Time (ps)	Fall Time (ps)	SNR
4700	4700	4700	0.00	0.0	0.0442	1.00E-09	371	371.5	16.15
4700	4900	4800	0.04	4.2	0.0442	9.98E-10	373.5	374.5	15.623
4700	5100	4900	0.08	8.2	0.044	9.99E-10	375.5	376.5	15.188
4700	5300	5000	0.12	12.0	0.0439	9.99E-10	377.5	378	14.685
4700	5500	5100	0.16	15.7	0.0437	9.98E-10	380	381	14.1923
4700	5700	5200	0.19	19.2	0.0434	9.99E-10	384	384.5	13.6157
4700	5900	5300	0.23	22.6	0.0432	1.00E-09	385.5	386.5	13.169
4700	6100	5400	0.26	25.9	0.0428	9.99E-10	389.5	391	12.5267
4700	6300	5500	0.29	29.1	0.0423	9.99E-10	393.5	395.5	11.914
4700	6500	5600	0.32	32.1	0.0418	9.98E-10	397.5	399.5	11.186
4700	6700	5700	0.35	35.1	0.041	1.00E-09	401	402.5	10.416
4700	6900	5800	0.38	37.9	0.0401	9.99E-10	410	412.5	9.584
4700	7100	5900	0.41	40.7	0.0387	9.99E-10	417.5	422.5	8.589
4700	7300	6000	0.43	43.3	0.0367	9.97E-10	430	436	7.477

Table 4.1: Single Collector Resistance Sweep

The jitter results are omitted from this table as the jitter values did not change by any more than negligible amounts as collector resistance mismatch increased. It is also worth noting that the eye width did not change, so the plot below is only for eye height.

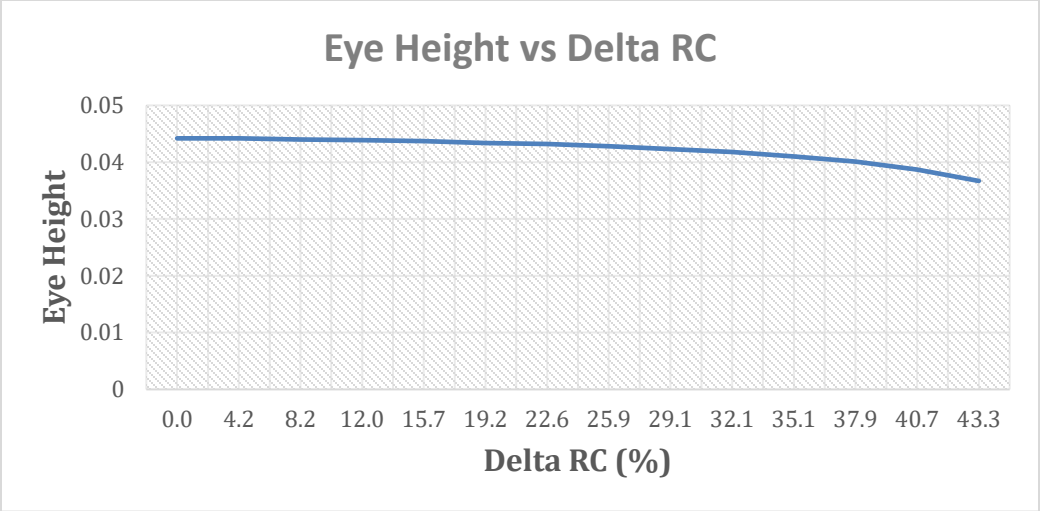

Figure 4.3: Eye Height vs Collector Resistance Change

Figure 4.3 above shows a slight decrease in eye height as the second collector resistance is increased. The gentle suggestion here is that the eye closes as collector resistance mismatch increases (worsens). This sweep will be improved for better mismatch characterization in the next experiment.

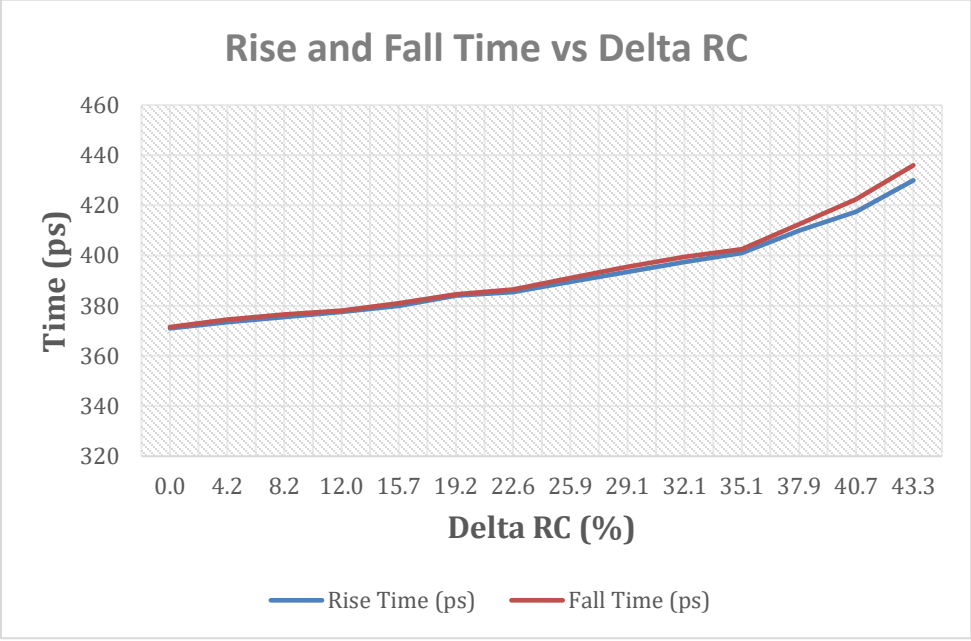

Figure 4.4: Rise and Fall Time vs Collector Resistance Change

Figure 4.4 above shows a fairly significant increase in rise and fall time as the second collector resistance increases, suggesting a negative correlation between collector resistance mismatch and rise and fall time.

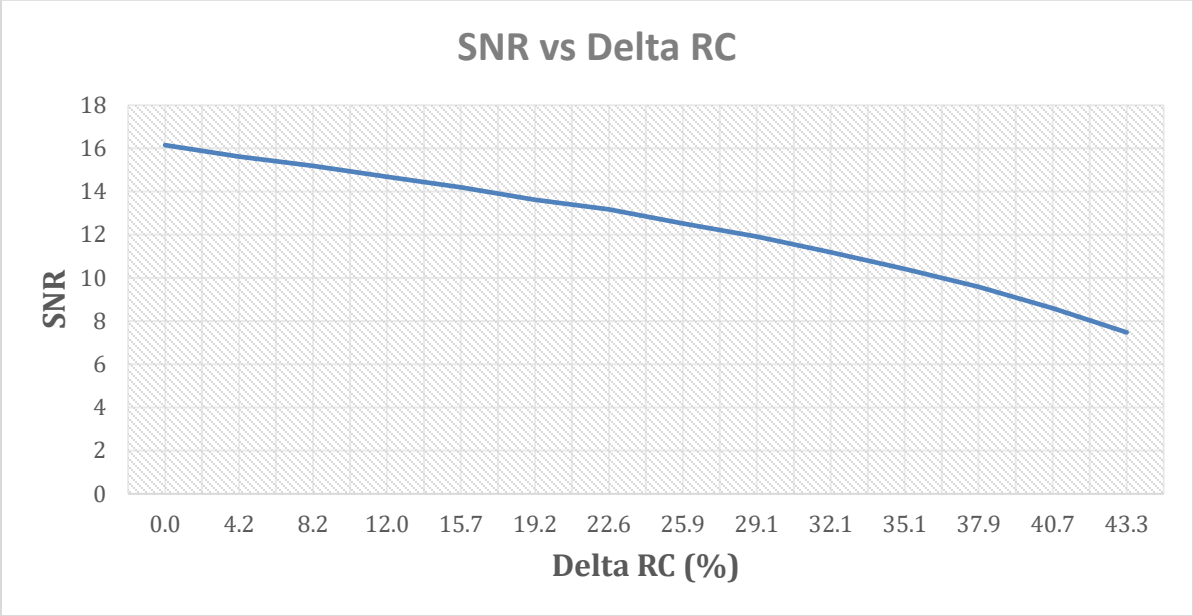

Figure 4.5: Signal-to-Noise Ratio vs Collector Resistance Change

Figure 4.5 shows that the signal-to-noise ratio declines significantly as collector resistance mismatch increases. This will also be repeated with better mismatch accuracy in the next sweeps.

A pitfall of the previous measurement is that it does not take into consideration the output parameter changes that occur as a function of either of the collector resistances simply increasing. The purpose of this thesis is to identify the effects of mismatch specifically, so the experiment was modified slightly to account for this. In the next section, one resistance will decrease while the other increases to negate any effects of increase or decrease on output parameters.

For this step, both collector resistances were initially set at the ideal 4.7k ohms. The first was then decreased by a step size of 200 ohms while the second was increased

by the same step size. The plots show changes in eye height, rise time, fall time, and signal-to-noise ratio as a function of the difference between the collector resistances.

RC1 (ohms)	RC2 (ohms)	RC	Delta RC	Delta RC (%)	Delta Eye Height	Delta Rise Time (%)	Delta SNR (%)
4700	4700	4700	0.000	0.0%	0.0%	0.0%	0.0%
4500	4900	4700	0.085	8.5%	0.0%	0.0%	0.4%
4300	5100	4700	0.170	17.0%	0.2%	0.4%	2.0%
4100	5300	4700	0.255	25.5%	0.7%	0.5%	3.1%
3900	5500	4700	0.340	34.0%	1.4%	0.7%	5.7%
3700	5700	4700	0.426	42.6%	1.8%	0.7%	7.5%
3500	5900	4700	0.511	51.1%	2.9%	1.1%	10.9%
3300	6100	4700	0.596	59.6%	4.1%	1.8%	14.8%
3100	6300	4700	0.681	68.1%	5.7%	2.3%	19.1%
2900	6500	4700	0.766	76.6%	7.7%	3.2%	24.3%
2700	6700	4700	0.851	85.1%	10.0%	4.7%	30.7%

Table 4.2: Collector Resistance Mismatch Sweep

Just as in the previous sweeps, a value for the delta in collector resistance (ΔR_C) is calculated to characterize the mismatch specifically. This is shown in Table 2 above. The output parameters have also been measured in a delta format. The end of the sweep shows a significant amount of collector resistance mismatch. Again, eye width and jitter have both been omitted as the changes are negligible or nonexistent.

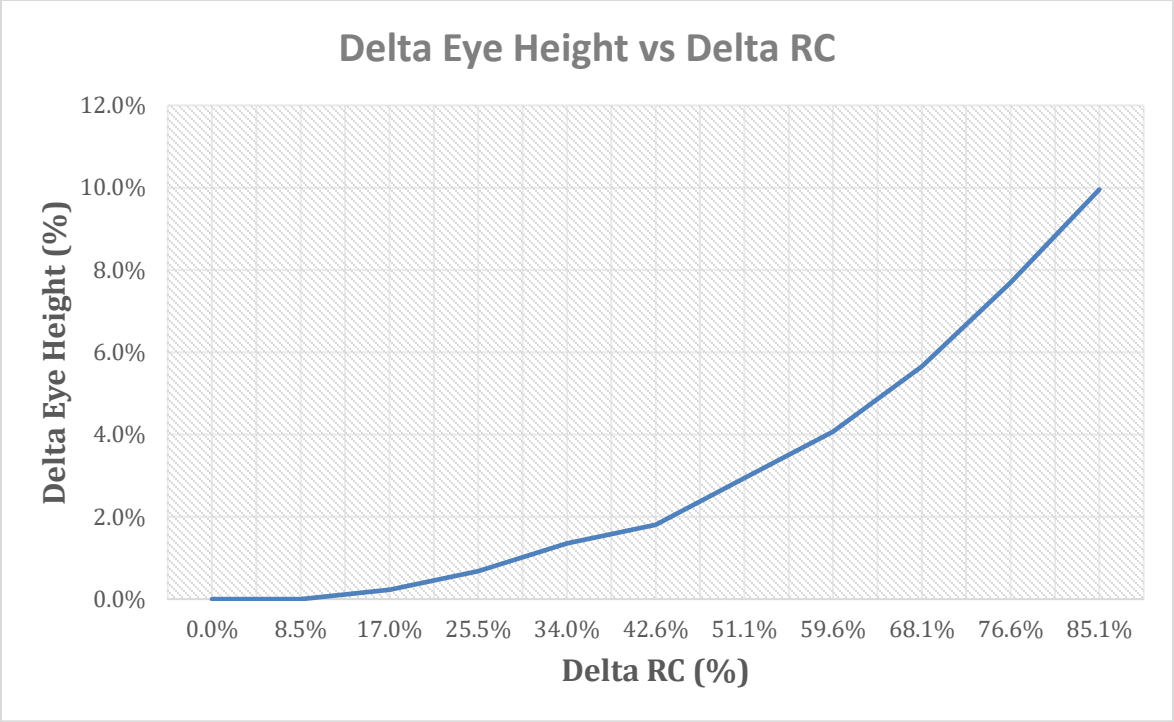

Figure 4.6: Delta Eye Height vs Collector Resistance Mismatch

The first output parameter measured is change in eye height, shown in Figure 4.6 above. This is measured as a function of actual mismatch in collector resistance. As it removes the effect of simply increasing collector resistance by moving the two in separate directions to cancel out, this is a significantly more accurate representation of the effects of mismatch. As the delta between collector resistances increases, delta eye height is increased and, therefore, eye opening is reduced. Greater collector resistance mismatch correlates to reduction in signal fidelity as seen through the eye pattern opening.

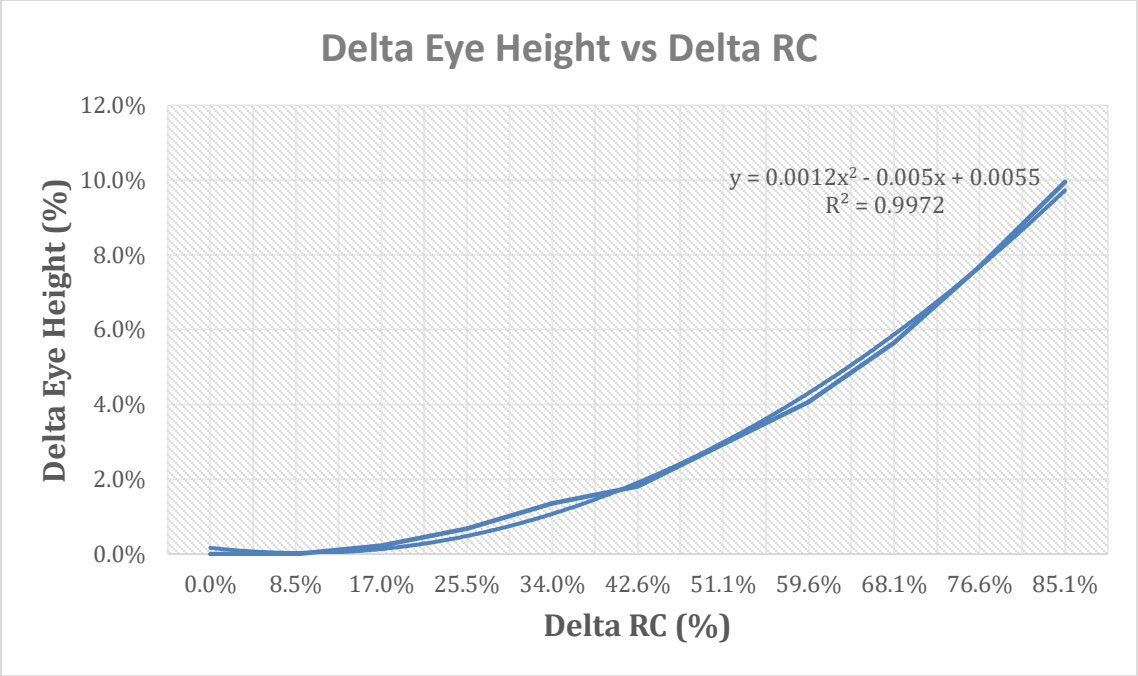

Figure 4.7 Eye Height vs R_C Curve Fitting

Figure 4.7 above is the same data as given in Figure 4.6, but the plot above has a second-order polynomial curve fit to the data. The relationship between eye height and rise time can be characterized by the following equation:

$$\Delta EyeHeight = 0.0012(\Delta R_C)^2 - 0.005(\Delta R_C) + 0.0055$$

As seen from the data above, a 50% mismatch in R_C can correspond to only 3% change in eye height, whereas 85% R_C mismatch equates to more than 10% eye height change. The collector resistance mismatch can be more than 25% before the eye height is reduced by even a single percentage point, and there appears to be effectively negligible eye height change before 15% R_C mismatch. This suggests a collector resistance mismatch tolerance of at least 10% for eye pattern height.

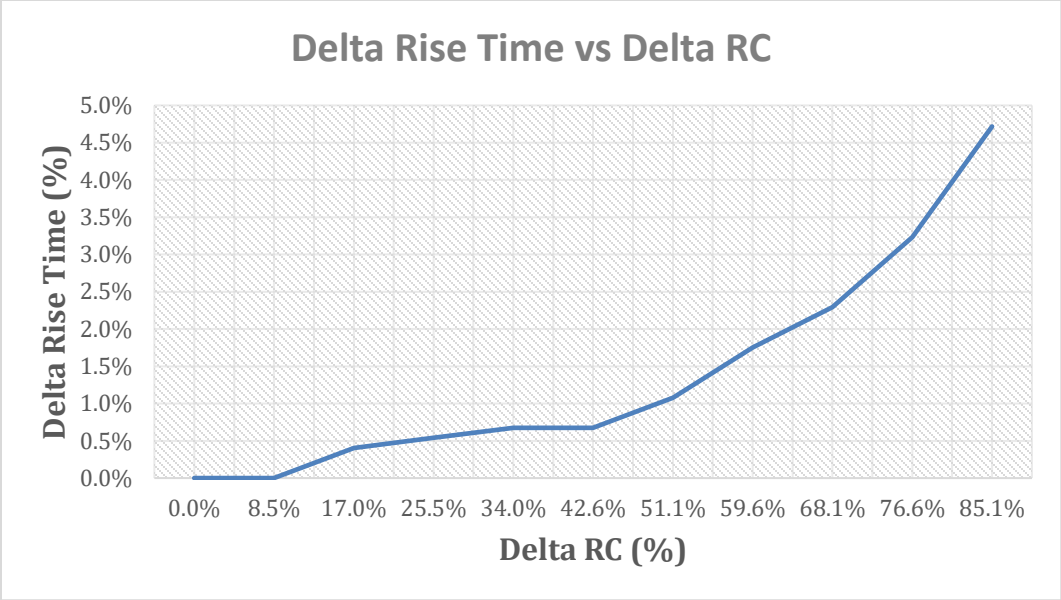

Figure 4.8: Rise and Fall Time vs Collector Resistance Mismatch

Figure 4.8 above shows an increase in rise time, as well as an increase in delta rise time, as collector resistance mismatch increases. As mismatch between collector resistances worsens, the signal swing and differential amplification becomes slower. This result was predicted previously in the method section of this thesis. One of the three parts of the time constant derived for this circuit involved the R_C value. While smaller than the R_E component, the R_C component was too large to neglect or omit. The speed of these amplifiers, as modeled by the time constant, is a function of the collector resistances.

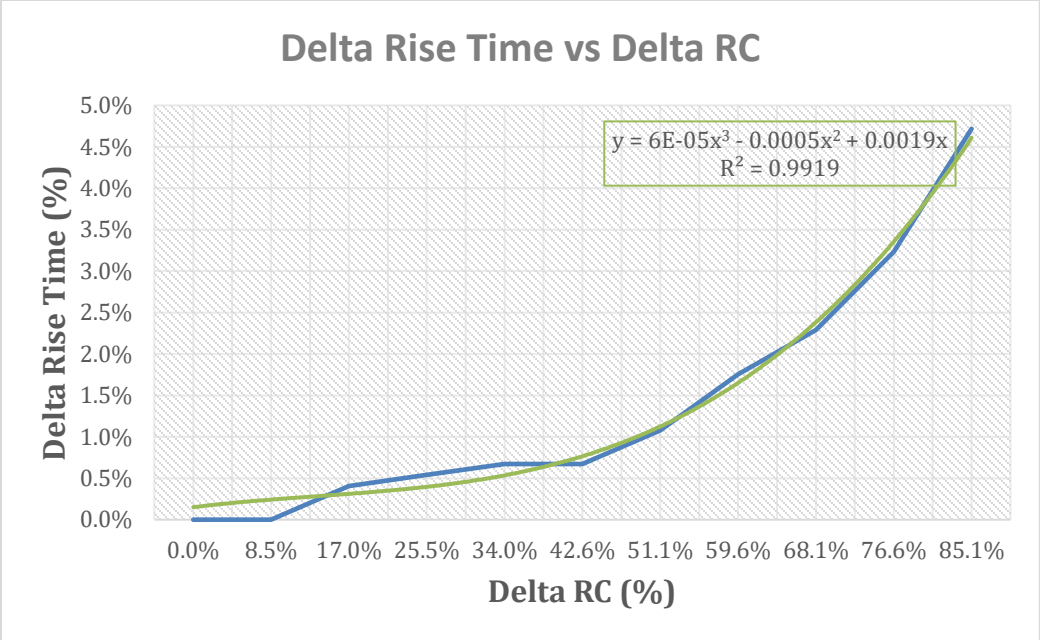

Figure 4.9 Rise Time vs R_E Curve Fitting

Figure 4.9 above shows the same plot as Figure 4.8, but with a third-order polynomial curve fit to the data. The relationship between change in rise time and change in collector resistance mismatch can be characterized by:

$$\Delta RiseTime = 0.00006(\Delta R_C)^3 - 0.0005(\Delta R_C)^2 + 0.0019(\Delta R_C)$$

The effect of collector resistance mismatch on rise time is fairly small, with an 85% mismatch corresponding to less than 5% rise time change. According to the sweep in this simulation, this parallel amplifier configuration can tolerate almost 50% collector resistance mismatch before seeing a 1% change in rise time.

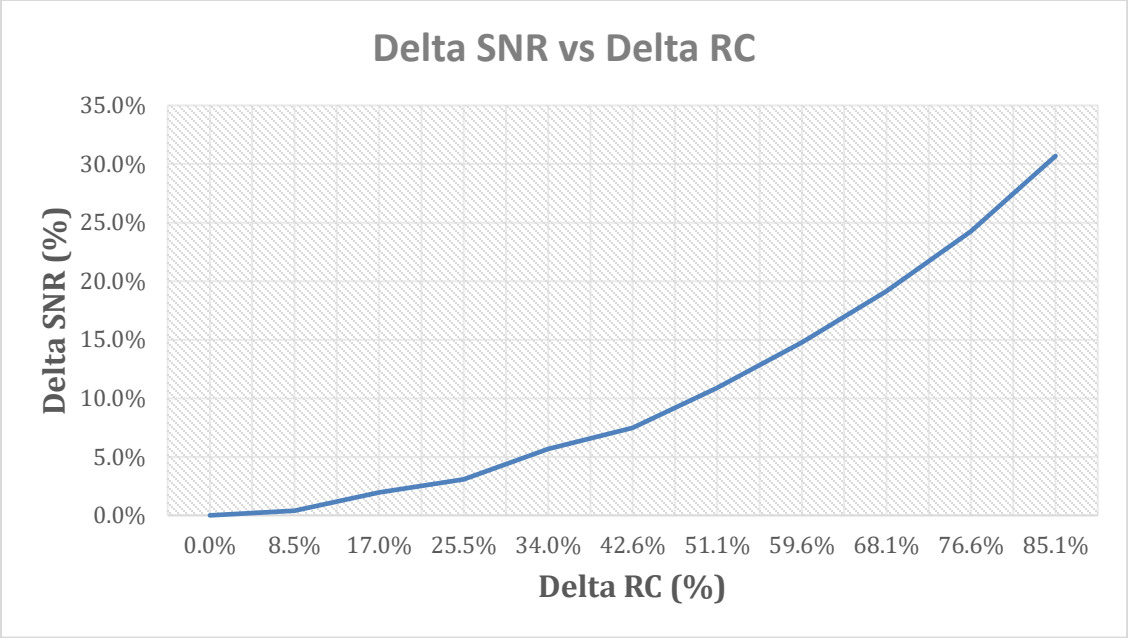

Figure 4.10: Signal-To-Noise Ratio Difference vs Collector Resistance Mismatch

Finally, Figure 4.10 above shows an increase in the delta signal-to-noise ratio (decrease in signal-to-noise ratio) as the collector resistances grow further apart. The one and zero levels become harder to differentiate as the collector resistance mismatch worsens. This can easily be traced to the eye height and rise time effects as well. As rise time increases, the side bit-crossings can vary. This along with reduction in eye height corresponds to a closing of the eye pattern, which can also be explained by a reduction in signal-to-noise ratio.

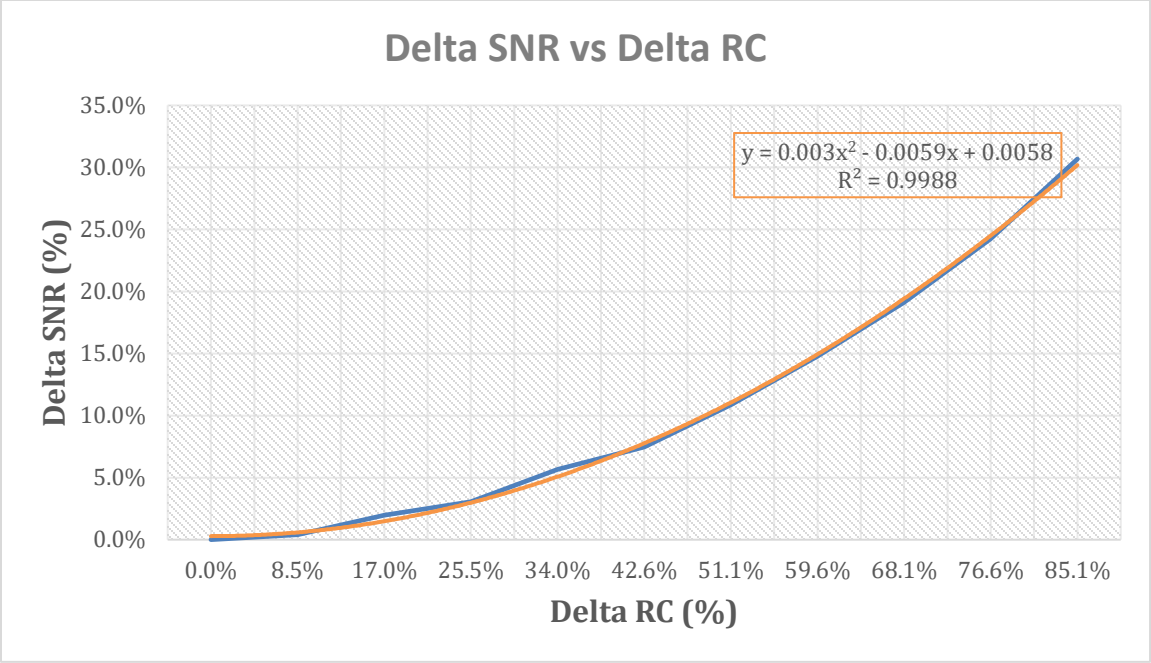

Figure 4.11: SNR vs R_C Curve Fitting

The plot in Figure 4.11 above is the same as the original SNR plot in Figure 4.10, but a second-order polynomial curve has been fit to the data. This relationship is characterized by the equation as follows:

$$\Delta SNR = 0.003(\Delta R_C)^2 - 0.0059(\Delta R_C) + 0.0058$$

Collector resistance mismatch seems to have a greater effect on SNR than on eye height or rise time. A mismatch of 85% can lead to reduction of signal-to-noise ratio on the order of 30%. From this data, the parallel amplifier configuration can tolerate a collector resistance mismatch of 10% before seeing much more than 1% reduction in signal-to-noise ratio.

This second version of the experiment shows results that are similar in form to the additional sweep, but far more accurate a representation of the effects of mismatch. We see here that the eye height decreases significantly as mismatch between the two collector resistances increases (worsens). There is a similar increase (worsening) in rise and fall

time as collector resistance mismatch increases. It is interesting to note that the signal-to-noise ratio decrease seems to be more severe with respect to the first experiment.

In the scope of this thesis, mismatch between the collector resistances of two amplifiers connected in parallel on a differential line seems to have a noteworthy effect on output parameters measured in an eye diagram.

4.2.3 Beta

The current gain of a BJT is denoted by beta. In the ADS BJT model, "Bf" corresponds to the ideal maximum forward beta value. The default value on the specific model used in this simulation is 115.98, while the ideal beta value used in most general calculations is 100. After learning from the resistance sweeps, beta will only be investigated from a mismatch perspective; the two beta values will be moved incrementally further apart. Both beta values are set at 115.98 for the first data point, then the first is decreased by a step size of 1 (rounding to start at 115) while second is increased by the same amount (rounding to 117 for simplicity). A metric was derived for characterizing mismatch percentage for the beta parameter as follows.

$$\Delta\beta_C = \frac{|\beta_1 - \beta_2|}{\beta}$$

$$\beta = \frac{\beta_1 + \beta_2}{2}$$

Bf1	Bf2	Beta	Delta Beta	**Delta Beta (%)**	Eye Height	Rise Time (ps)	Fall Time (ps)	SNR	Delta SNR (%)
115.98	115.98	115.98	0.0000	**0.0%**	0.0442	371	371.5	16.14842	0.00%
115	117	116	0.0172	**1.7%**	0.0442	371	371.5	16.14842	0.00%
114	118	116	0.0345	**3.4%**	0.0442	371	371.5	16.15194	0.02%
113	119	116	0.0517	**5.2%**	0.0442	371	371.5	16.15453	0.04%
112	120	116	0.0690	**6.9%**	0.0442	371	371.5	16.16394	0.10%
111	121	116	0.0862	**8.6%**	0.0442	371	371.5	16.16867	0.13%
110	122	116	0.1034	**10.3%**	0.0442	371	371.5	16.16968	0.13%
109	123	116	0.1207	**12.1%**	0.0442	371	371.5	16.17053	0.14%
108	124	116	0.1379	**13.8%**	0.0442	371	371.5	16.17053	0.14%
107	125	116	0.1552	**15.5%**	0.0442	371	371.5	16.17499	0.16%
106	126	116	0.1724	**17.2%**	0.0442	371	371.5	16.17488	0.16%

Table 4.3: Beta Mismatch Sweep

Table 4.5 above shows the swept beta values and corresponding output parameter changes, in addition to including this new Delta Beta value. Rise time, fall time, and eye height don't change by any real amounts as a function of beta, so the only change plotted below is signal-to-noise-ratio.

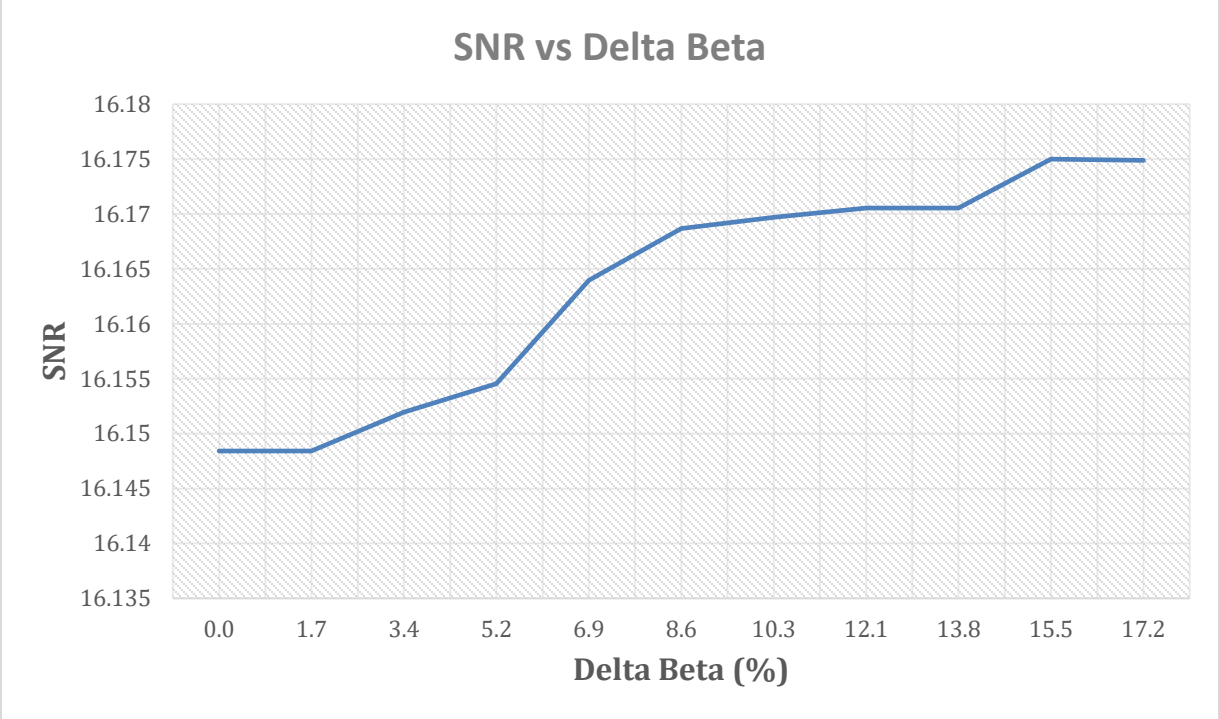

Figure 4.12: Signal-to-Noise Ratio vs Beta Mismatch

As with the collector resistance sweeps, eye width and jitter don't change by any measurable amount to note. For the beta changes, however, it is interesting to note that the eye height and rise and fall time don't vary by more than negligible quantities. The only measurable change is signal-to-noise ratio, with significantly smaller changes than seen during the resistance sweeps. The plot of SNR vs beta mismatch in Figure 4.12 shows a trend of SNR increasing as beta mismatch increases. For the sake of clarity, this data will be displayed in a slightly more precise form below.

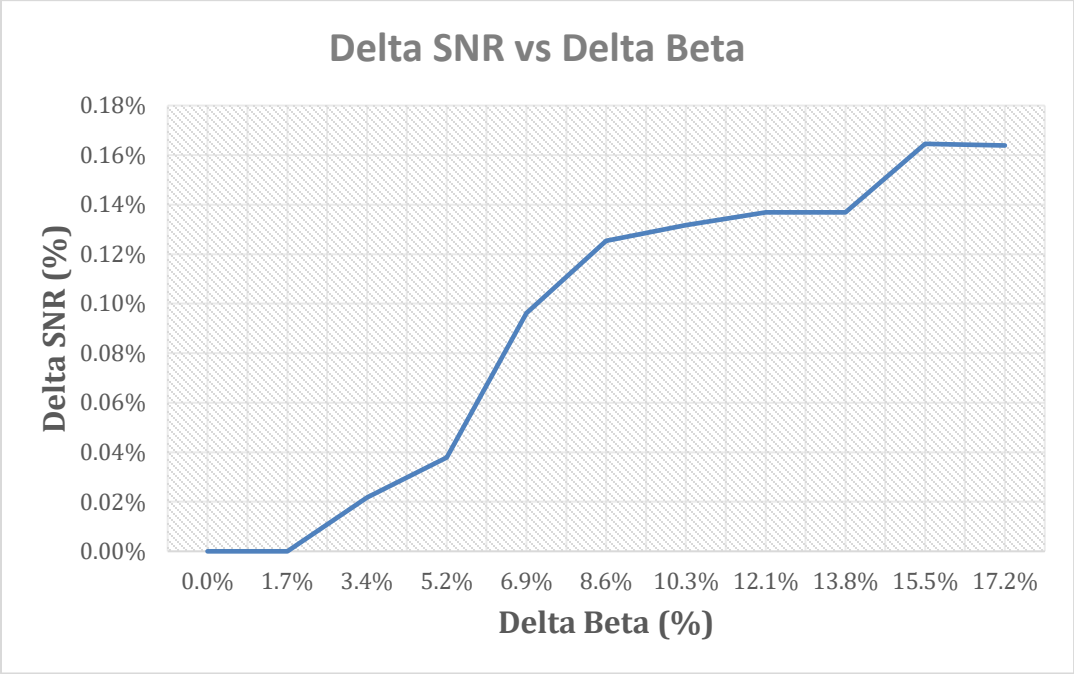

Figure 4.13: Delta SNR vs Delta Beta

Figure 4.13 above shows a clearer picture of the effect of beta mismatch on signal-to-noise ratio. Here the presentation is Delta SNR as a function of Delta Beta. A curve has been fitted to this data in the plot below.

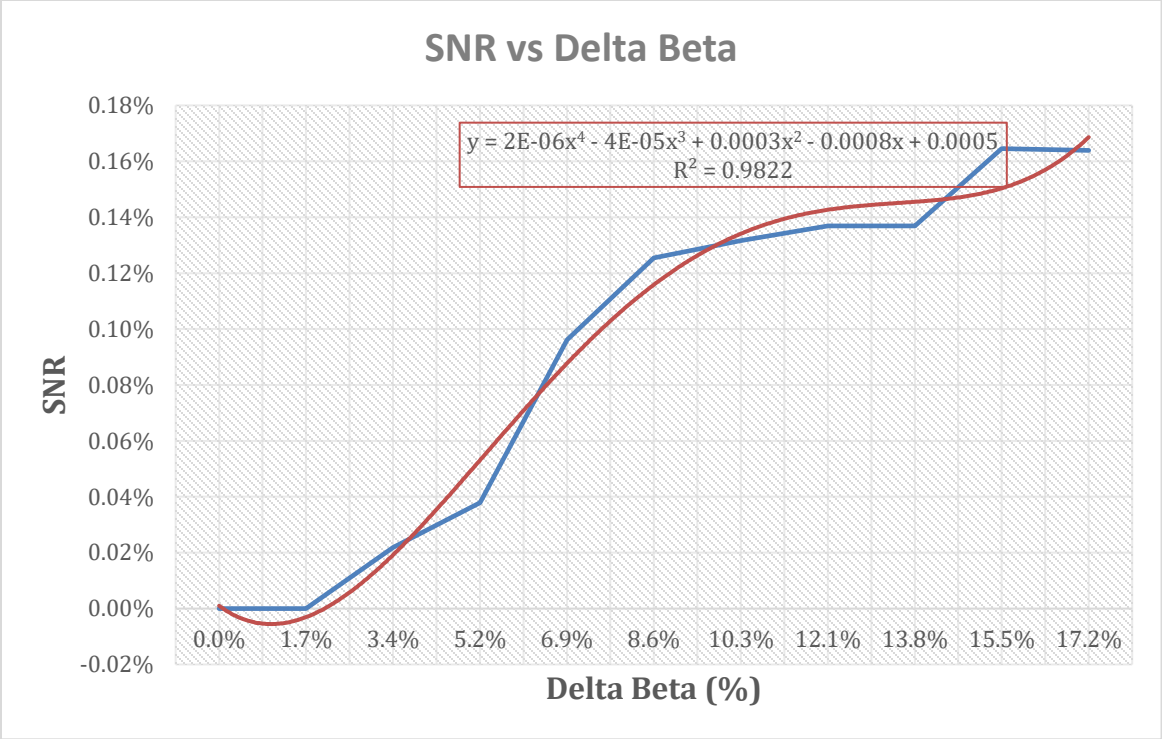

Figure 4.14: SNR vs Beta Curve Fitting

Figure 4.14 is the same data as in figure 4.13, but with a fourth-order polynomial curve fit to the data. The relationship between signal-to-noise ratio and beta mismatch can be characterized by the following equation:

$$\Delta SNR = 0.000002(\Delta Beta)^4 - 0.00004(\Delta Beta)^3 + 0.0003(\Delta Beta)^2 - 0.0008(\Delta Beta) + 0.0005$$

This equation is slightly more complex than those from the collector resistance sweeps. While SNR was the only parameter to change by more than negligible numbers as a function of beta mismatch, the plot above shows that, as beta mismatch approaches 20%, the decline in SNR is on the order of 0.2%, a fifth of a percentage point. This small amount of correlation could be due to various errors or imprecisions in the model and simulation software and will therefore be considered not statistically significant in this thesis. Under the scope of this thesis, beta mismatch between two parallel amplifiers appears to have no known and significant effect on eye diagram output parameters.

4.3.3 Emitter Resistance

The final parameter swept was the emitter resistance. As the emitter resistance is the only value used in the dominant time constant (calculated in the method section), this will be the most useful and descriptive simulation. The starting value for both, and the value at which the top amplifier was held, is 470 Ohms. The bottom emitter resistance was swept from 470 to 730 with a 20-ohm step size. For each of these collector resistance pairs, a value of ΔR_E (Delta RE) is calculated and given as a percentage change value.

RE1 (ohms)	RE2 (ohms)	RE	Delta RE	**Delta RE (%)**	Eye Height	Eye Width	Rise Time (ps)	Fall Time (ps)	SNR
470	470	470	0.000	**0.0**	0.0442	1.00E-09	371.5	372.5	16.0854
470	490	480	0.042	**4.2**	0.0442	9.98E-10	372.5	373	16.25723
470	510	490	0.082	**8.2**	0.0442	9.99E-10	370	371.5	16.48318
470	530	500	0.120	**12.0**	0.0443	9.99E-10	370	370.5	16.6956
470	550	510	0.157	**15.7**	0.0442	9.98E-10	369.5	370.5	16.87441
470	570	520	0.192	**19.2**	0.0443	9.99E-10	367.5	369	17.04396
470	590	530	0.226	**22.6**	0.0442	1.00E-09	367	367.5	17.1959
470	610	540	0.259	**25.9**	0.0441	9.99E-10	367	367	17.3411
470	630	550	0.291	**29.1**	0.0442	9.99E-10	366.5	368	17.58807
470	650	560	0.321	**32.1**	0.0441	9.98E-10	365.5	366.5	17.64766
470	670	570	0.351	**35.1**	0.044	1.00E-09	365	365.5	17.79975
470	690	580	0.379	**37.9**	0.044	9.99E-10	364.5	365.5	17.83424
470	710	590	0.407	**40.7**	0.044	9.99E-10	365.5	366.5	17.95481
470	730	600	0.433	**43.3**	0.0439	9.97E-10	364.5	365.5	17.9647

Table 4.4: Single Emitter Resistance Sweep

Using the EyeDiff_Probe component/tool in ADS, the eye height and width, rise and fall times, jitter, and signal-to-noise ratio were all measured at each step. Table 3 above shows the results and details of this sweep, including the calculated ΔR_E values. Similar to the collector resistance sweep, the eye width and jitter values for the emitter resistance sweep are small enough to be negligible, with any simulated measurements being likely attributed to random noise and computational nonidealities.

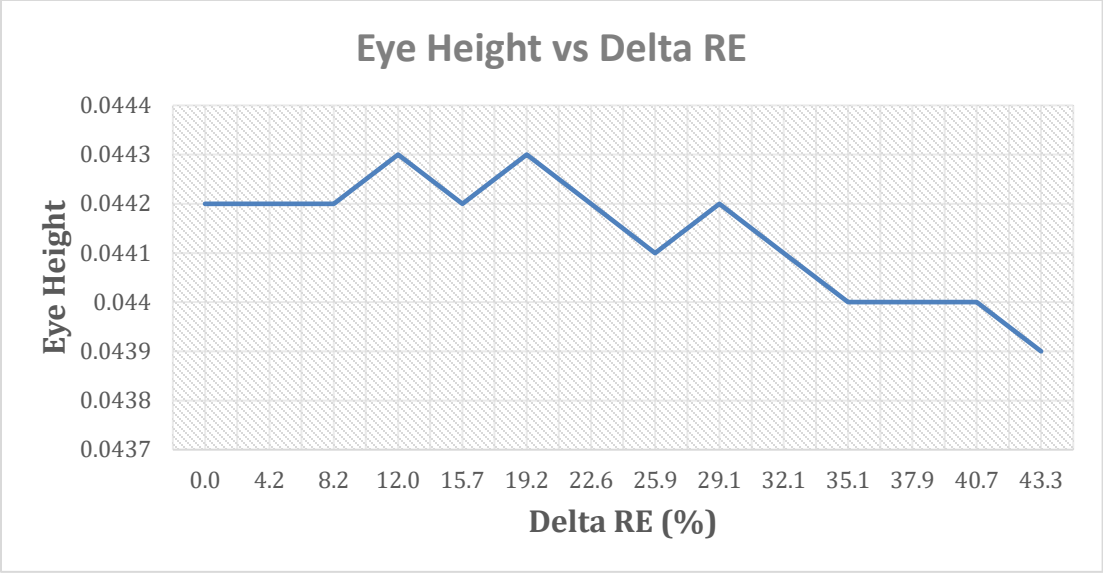

Figure 4.15: Eye Height vs Emitter Resistance Change

Figure 4.15 above shows the first sweep, measuring change in eye height as the second emitter resistance is increased and the first remains fixed. The correlation between eye height and Delta R_E is not overly conclusive. There is a general trend of reduction in eye height as emitter resistance mismatch worsens. Like the collector resistance sweep, however, this is also not the best isolation of mismatch effects and will be improved upon in the next section.

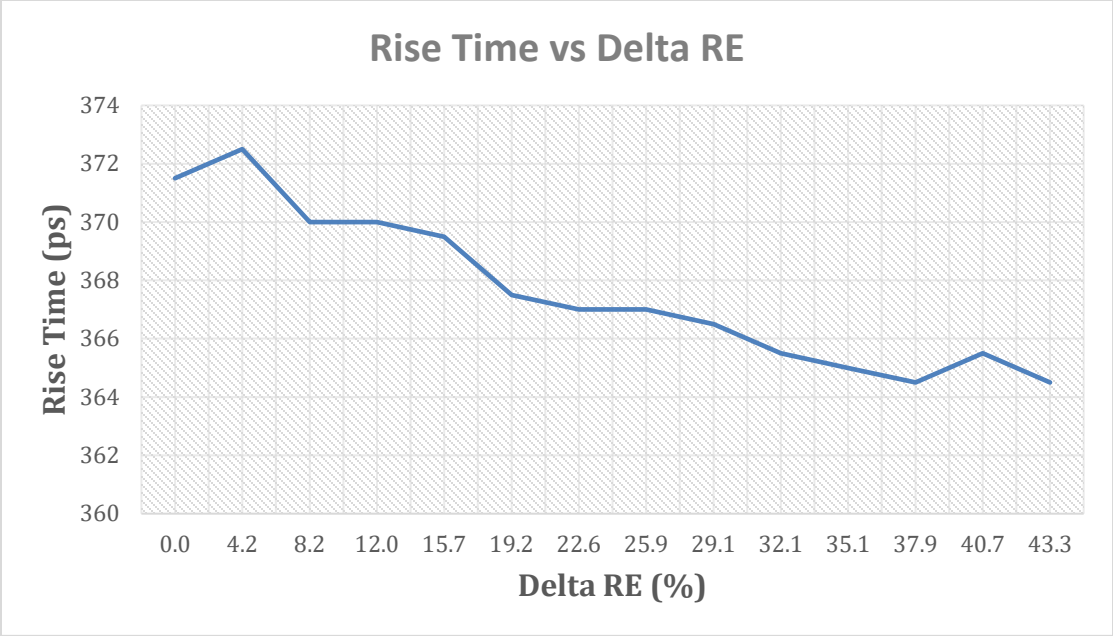

Figure 4.16: Rise time vs Emitter Resistance Change

There is, however, more significant effect of mismatch on Rise time as seen from Figure 4.16 above. Note that fall time is almost identical, but because of the similarities this section will isolate rise time alone. There is a moderate decrease in rise time as a function of emitter resistance mismatch.

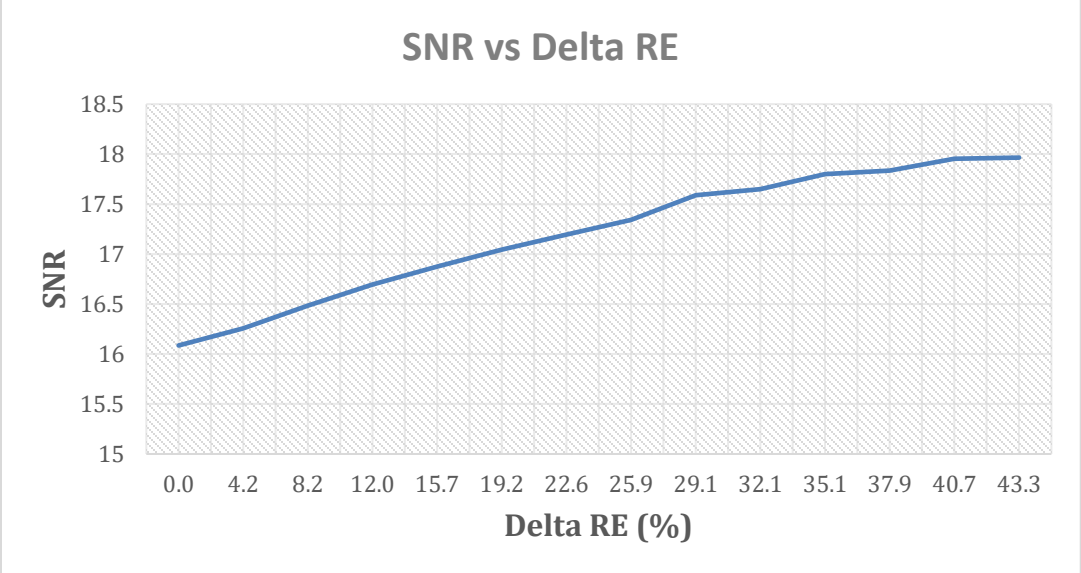

Figure 4.17: Signal-to-Noise Ratio vs Emitter Resistance Change

This simulation yields results of slightly more interest than the collector resistance sweeps. First, note that the eye height as a function of changing the second emitter resistance almost seems to have no useful pattern. This is an unexpected response and seems to be a misdirection, most likely an issue with initial biasing of the circuit. Second, the rise time actually decreases as the second emitter resistance increases, which also seems to suggest that there was a slight problem with optimal biasing of the circuit. This is confirmed one final time in the signal-to-noise ratio plot, with SNR increasing as the second emitter resistance increases.

The red herring here would be to assume that emitter resistance mismatch results in increased signal to noise ratio and faster rise times, which wouldn't make much sense. Similar to the collector resistance, however, it is safe to assume some of the pattern is not specifically attributed to mismatch, but instead just a result of one of the amplifiers seeing increasing emitter resistance. Therefore, once again, the emitter resistance will be swept in opposite directions on both amplifiers. Both will start at 470 ohms, then the top amplifier will decrease by a step size of 20 ohms while the bottom increases by 20 ohms per step. The following sweeps will attempt to accurately show the effects of emitter resistance mismatch between the two parallel amplifiers. Just as in the previous sweeps, a value for the delta in emitter resistance (ΔR_E) is calculated to characterize the mismatch specifically. This is shown in Table 3 below. The end of the sweep shows a significant amount of emitter resistance mismatch, on the order of 85%.

RE1 (ohms)	RE2 (ohms)	RE	Delta RE	**Delta RE (%)**	Eye Height	Delta Eye Height	Rise Time (ps)	Delta Rise Time (%)	SNR	Delta SNR
470	470	470	0.000	**0.0%**	0.0442	0.00%	371.5	0.0%	16.0854	0.0%
450	490	470	0.085	**8.5%**	0.0442	0.00%	372	0.1%	16.02884	0.4%
430	510	470	0.170	**17.0%**	0.044	0.45%	373	0.4%	15.7964	1.8%
410	530	470	0.255	**25.5%**	0.044	0.45%	374.5	0.8%	15.56201	3.3%
390	550	470	0.340	**34.0%**	0.0437	1.13%	375	0.9%	15.05308	6.4%
370	570	470	0.426	**42.6%**	0.0433	2.04%	378	1.7%	14.52605	9.7%
350	590	470	0.511	**51.1%**	0.0429	2.94%	381.5	2.7%	13.75871	14.5%
330	610	470	0.596	**59.6%**	0.0422	4.52%	384.5	3.5%	12.81312	20.3%
310	630	470	0.681	**68.1%**	0.041	7.24%	393.5	5.9%	11.37721	29.3%
290	650	470	0.766	**76.6%**	0.0389	11.99%	406	9.3%	9.44346	41.3%
270	670	470	0.851	**85.1%**	0.0357	19.23%	416.5	12.1%	8.53867	46.9%

Table 4.5: Emitter Resistance Mismatch Sweep

Again, the eye width and jitter changes have been omitted as they are negligible values too small to be accurately measured. In the eye height plot below it is shown that the relationship between eye height and emitter resistance difference is actually quite exponential. As the difference between the two emitter resistance values increases, the height of the eye diagram decreases exponentially.

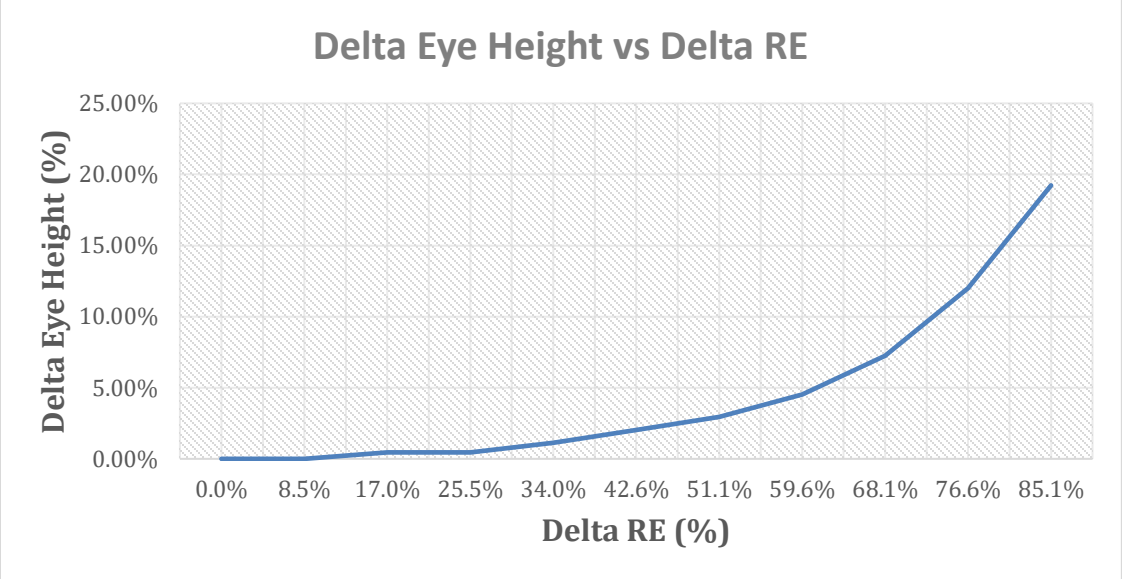

Figure 4.18: Delta Eye Height vs Delta Emitter Resistance Mismatch

The eye height change as a function of emitter resistance mismatch is shown in Figure 4.18 above. The shows a general trend of eye height increase as emitter resistance mismatch increases.

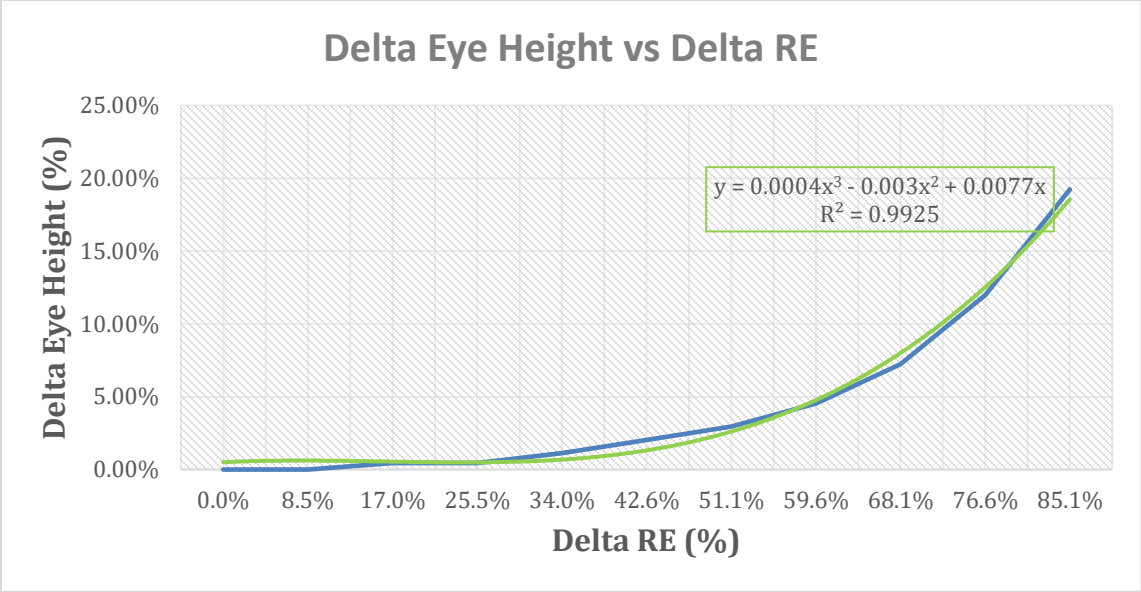

Figure 4.19: Eye Height vs R_E Curve Fitting

Taking the plot from Figure 4.18 one step further, Figure 4.19 presents the same data with a third-order polynomial curve fit. The relationship between change in eye height and emitter resistance mismatch is given as follows:

$$\Delta EyeHeight = 0.0004(\Delta R_E)^3 - 0.003(\Delta R_E)^2 + 0.0077(\Delta R_E)$$

As shown in this curve fitting, the relationship between eye height and emitter resistance mismatch is exponential. At 90% mismatch between emitter resistances there is a change in eye height of almost 20%. For this parallel amplifier configuration, the eye pattern can tolerate an emitter resistance mismatch of 25% before seeing a single percentage change in eye height.

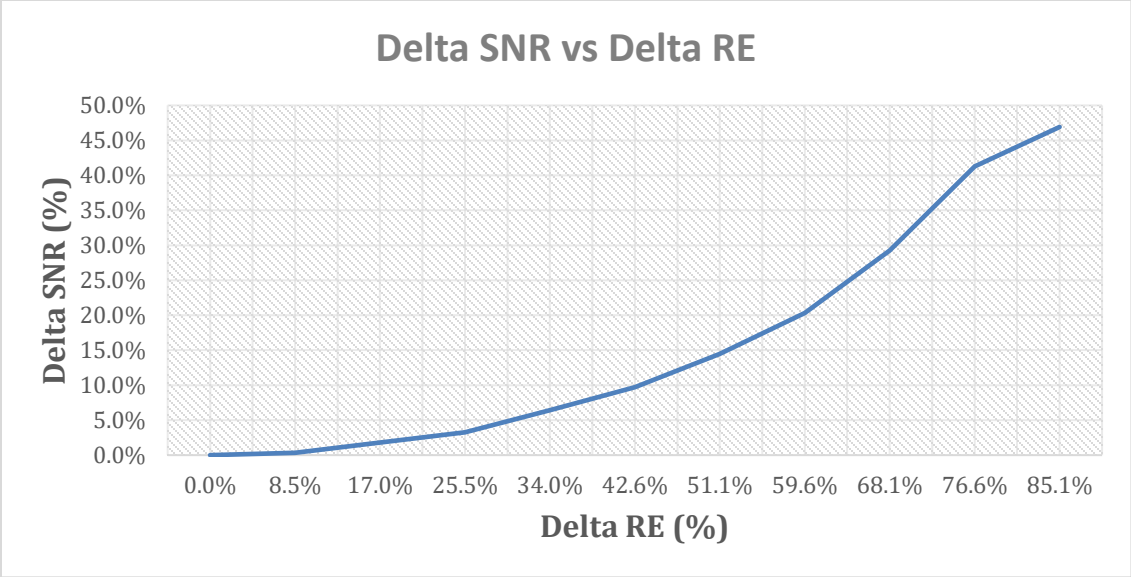

Figure 4.20: Delta Signal-to-Noise Ratio vs Emitter Resistance Mismatch

The SNR changes as a function of emitter resistance mismatch are very similar to that of collector resistance mismatch. As the mismatch in emitter resistance increases, signal-to-noise ratio decreases.

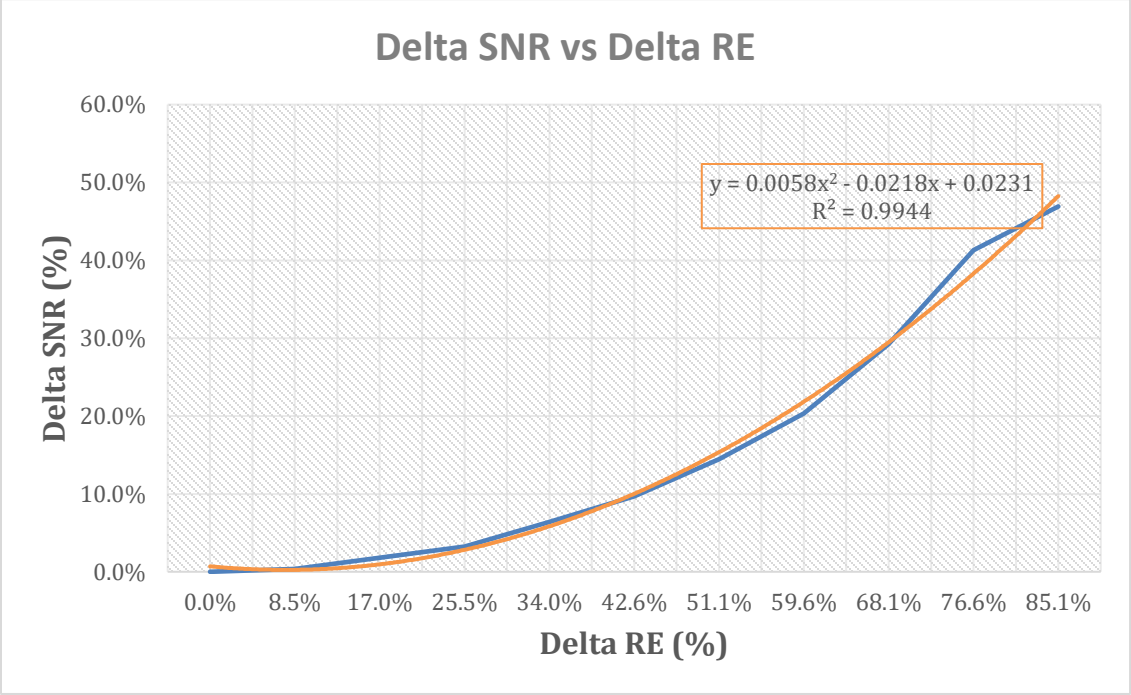

Figure 4.21: SNR vs R_E Curve Fitting

Figure 4.21 above shows the same plot as Figure 4.20 with a second-order polynomial curve fit to the data. The relationship between change in SNR and emitter resistance mismatch is given by the equation below:

$$\Delta SNR = 0.0058(\Delta R_E)^2 - 0.0218(\Delta R_E) + 0.0231$$

The previous plots show that the mathematical relationship between delta SNR and delta R_E is fairly smooth and exponential. Emitter resistance mismatch also appears to have a greater effect on signal-to-noise ratio than on eye height. At 85% mismatch between emitter resistances, there is almost 50% decrease in signal-to-noise ratio. It becomes far harder to distinguish the signal as the emitter resistances of the parallel amplifiers grow further apart. This design can tolerate a 10% mismatch in emitter resistance before seeing a 1% decrease in signal-to-noise ratio.

The most significant and useful result of this sweep is the rise time plot shown below. This shows a somewhat exponential relationship between rise time of the eye diagram and emitter resistance mismatch.

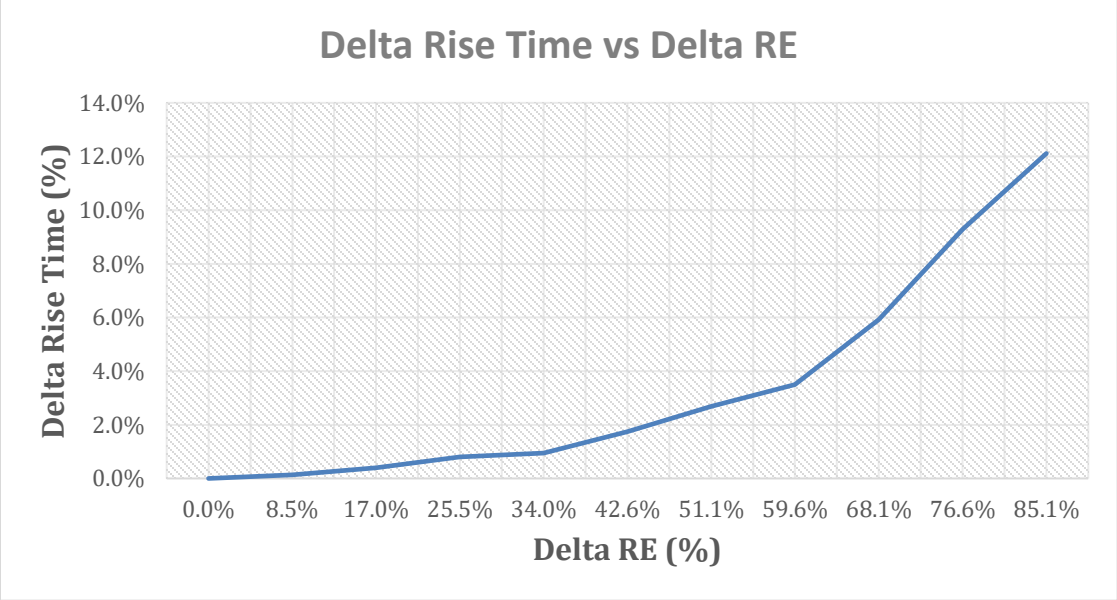

Figure 4.22: Delta Rise Time vs Delta R_E

Figure 4.22 above shows the most concrete relationship between rise time of the amplifier circuit and mismatch in the emitter resistances. This relationship is exponential, with an increase in the mismatch between emitter resistances resulting in an increase in rise time.

Mismatch between emitter resistances on two amplifiers connected in parallel on a differential line appears to have measurable and significant effects on output parameters as measured with an eye diagram.

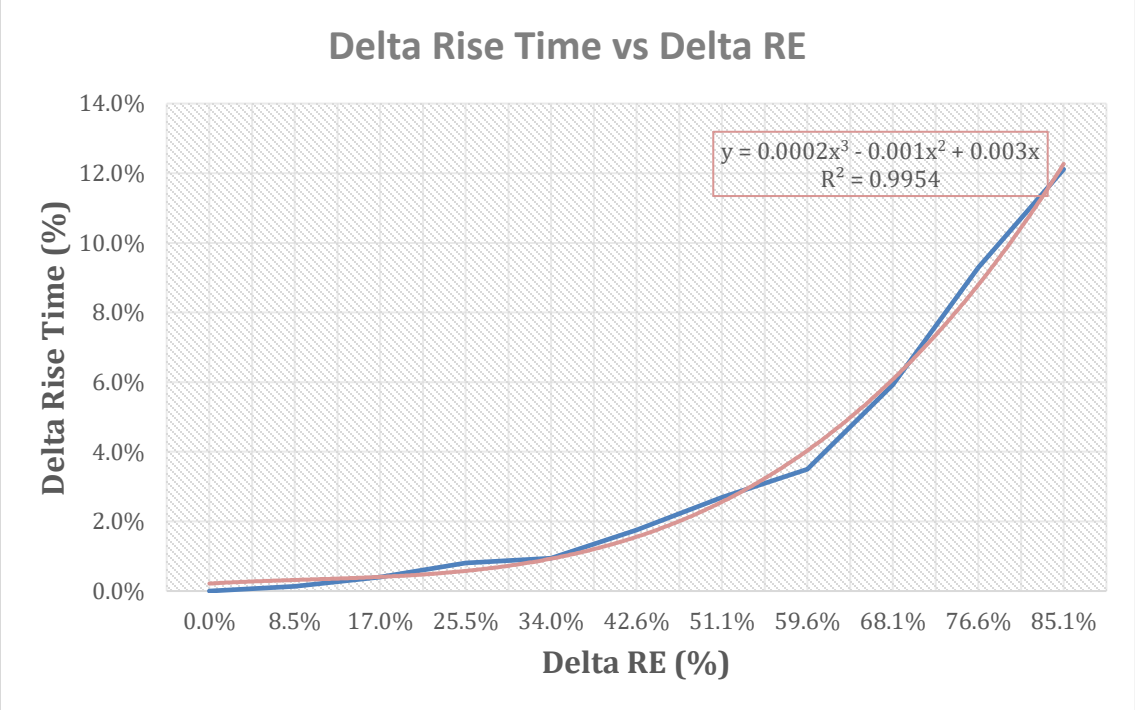

Figure 4.23 Rise Time vs R_E Curve Fitting

Figure 4.23 above shows the delta rise time vs delta R_E plot from before with a third-order polynomial curve fit to the data. This gives a relationship between delta rise time and delta R_E as follows:

$$\Delta RiseTime = 0.0002(\Delta R_E)^3 - 0.001(\Delta R_E)^2 + 0.003(\Delta R_E)$$

This relationship is slightly weaker than that of emitter resistance with eye height or signal-to-noise ratio. At an emitter resistance mismatch of 80% there is only about 10% change in rise time. While smaller than the other output parameters, this is no small amount of correlation. This parallel amplifier design can tolerate about 25% mismatch in emitter resistance to keep the rise time increase below 1%.

4.3.4 Emitter Resistance Theoretical vs Simulation

Section 3.5.4 of the Method outlined the use of open-circuit time-constants to model and derive the projected time constant for this amplifier. It is now practical to compare the predicted theoretical values of the circuit model to actual simulated values from the ADS eye diagram utility. Shown below are the time constant equations from the Method section.

$$\tau = \frac{47.6R_E}{47.6+R_E}(2.87\times10^{-12}) + \frac{1000R_C}{1000+R_C}(14.7\times10^{-15}) + \frac{1000R_C}{1000+R_C}(1\times10^{-12})$$

$$f(t) = 1 - e^{\frac{-t}{\tau}}$$

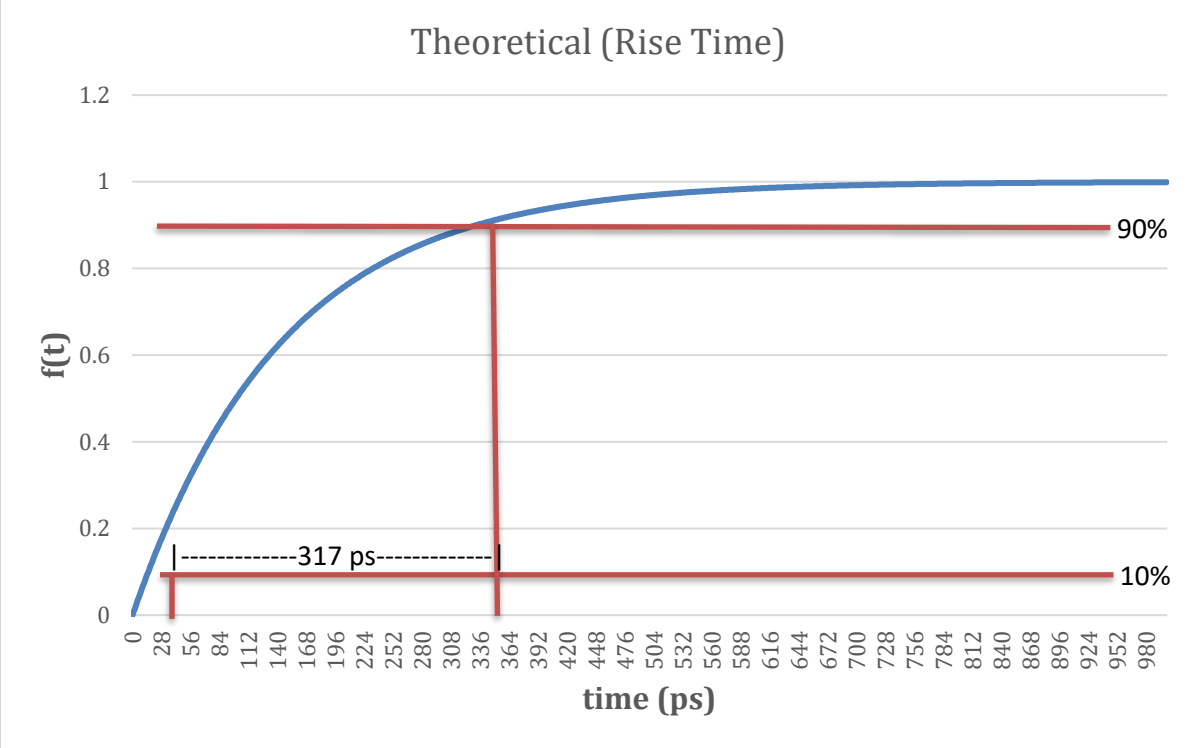

Figure 4.24: Theoretical Rise Time Plot

Figure 4.24 above shows a plot of the exponential rise time function, where τ has been calculated using all default values from the ADS design as given in the snapshot of the table seen below.

RC	RE	CBE	CCB	CL		**TCBE**	TCCB	TCL	T
4700	470	2.87E-12	1.47E-14	1.00E-14		**1.24E-10**	1.21E-11	8.25E-12	1.444E-10

In this modeled rise time plot, the "final" value is an asymptote at 1, this will be considered equivalent to the high voltage level in the eye diagram. The rise time boundaries of 10% and 90% have been added to Figure 4.18, giving an approximate theoretical rise time of 317 ps.

Theoretical Rise Time	**Simulated Rise Time**
317 ps	371 ps

The theoretical and simulated rise times given above are calculated and measured with default values across the board (R_E = 470 Ω, R_C = 4.7 kΩ). The rise time in the

simulation is expected to be higher than the theoretical calculation. The simulation uses a fairly complex transistor model with more than 30 distinct parameters, ranging from temperature coefficients to early voltage. For this reason it is a far more accurate representation of the real-world circuit performance, which will always be slower (longer rise and fall time) than the ideal theoretical value.

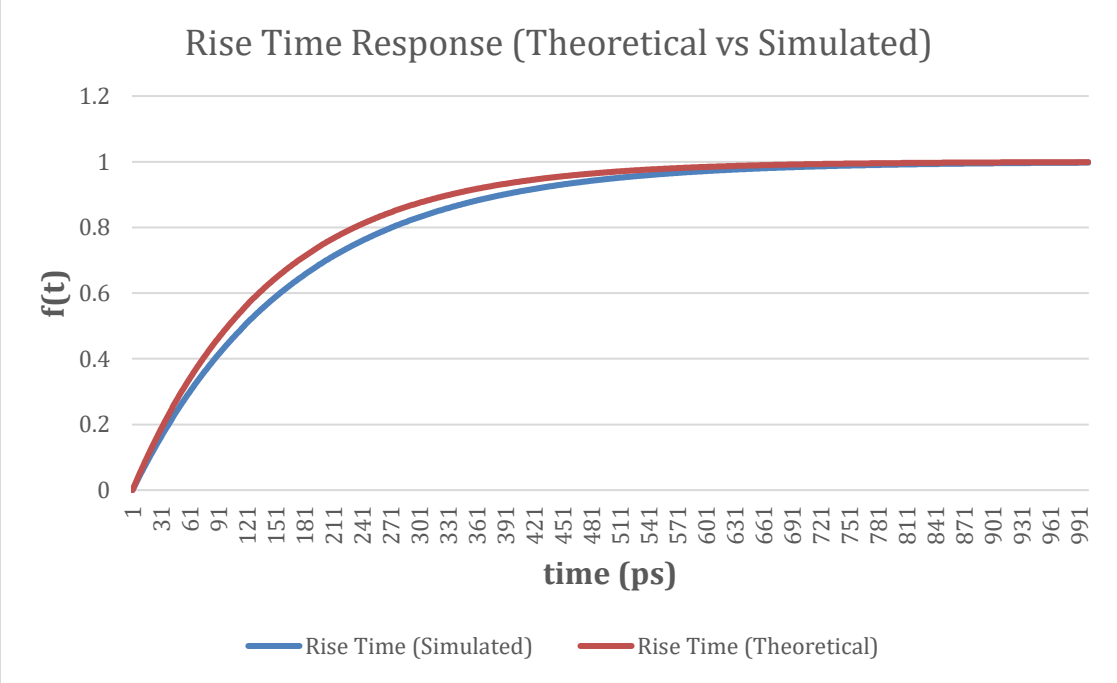

Figure 4.25: Theoretical vs Simulated Rise Time

In Figure 4.25 above, the rise time impulse plot from the theoretical derivation is overlayed with the simulated rise time. As can be seen in this graph, the model created for the ideal case was a reasonably good approximation of the rise time response of the amplifier circuit, and the ADS simulation verifies the accuracy of the model.

4.3.5 Bit Clarity and Voltage Level

Proper function of a digital signal, specifically a clock signal, relies heavily on the ability to distinguish the zero/low and one/high voltage levels to maintain a steady and accurate bitstream of 1s and 0s. A cornerstone of this process is that the signal is able to

reach the high voltage level quickly enough, and that it is able to maintain the high level for some amount of time for the bit to be processed and distinguished.

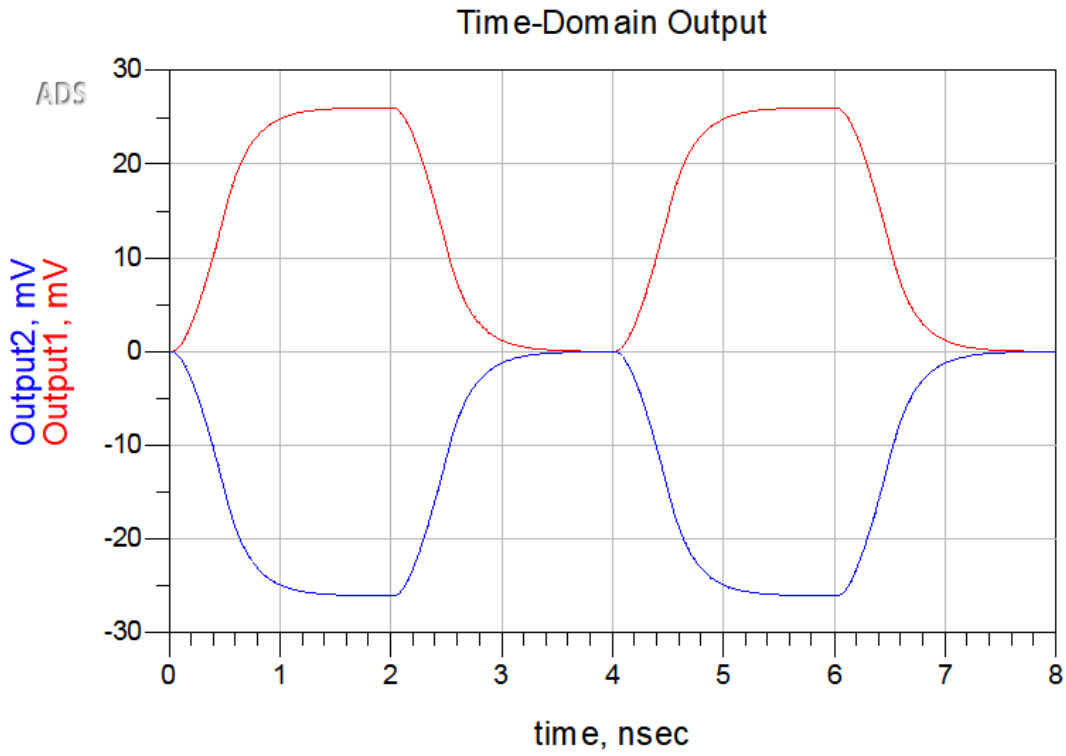

Figure 4.26: Time-Domain Output to Show Rise Time and "On" Time

Figure 4.26 above shows the output swing of both halves of the differential signal after being amplified. This time-domain simulation is run in Advanced Design System on the same parallel amplifier circuit used in the rest of the results section. As rise time and fall time increase – a phenomenon and effect that has been seen in this thesis as a result of mismatch – there is less available time for the signal to spend "high". In Figure 4.26 above, the signal period is 4 ns, with 2 ns reserved for the "on" cycle. The figure shows roughly 1 ns of "high" time during which the 1-bit can be detected. An extra 250 ps on both rise time and fall time will dramatically reduce the clarity and distinction between

low and high voltage levels. This is characterized for this specific parallel amplifier circuit design below.

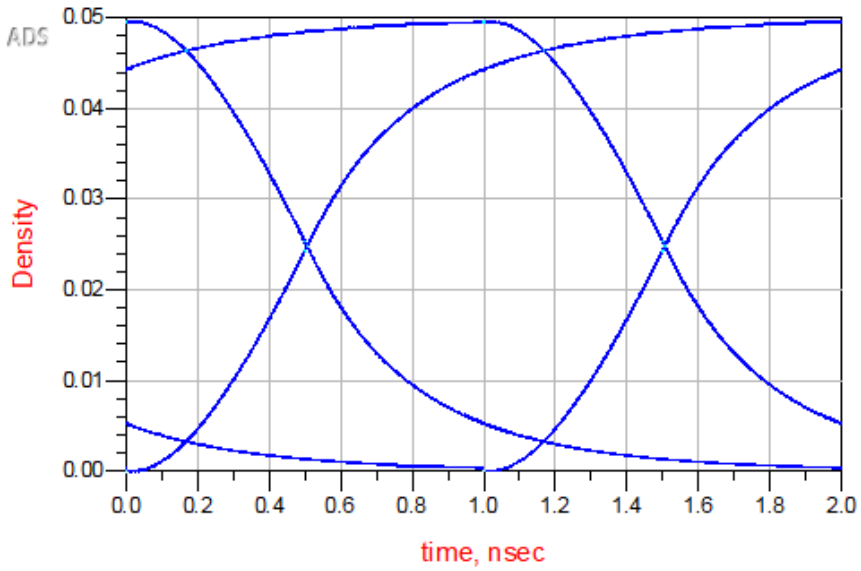

Figure 4.27: Slow Rise Time Example

Figure 4.27 above shows the eye diagram simulation window with significantly bad emitter resistance mismatch (~85%). It can be seen from this figure that, at this level of mismatch, the signal takes more than 1000ps to even begin levelling off. This combined with the similarly increased fall time will remove any flat high voltage-level time.

For the sake of this thesis, an assumption will be made that the required “on” time for the 250MHz digital clock signal is 400ps to achieve adequate bit accuracy and distinction. As the fall time has increased in near perfect symmetry with rise time, rise time and fall time will be considered identical. Assuming this 400ps taken from the 1000ps on time in the optimized amplifier design, the remaining 600ps would require an increase in rise time of more than 300ps to reduce bit clarity. For this design, rise time increase of 300ps would be a nearly 100% increase, which would require emitter

resistance mismatch on the order of 200%, which is not likely in real world amplifier ICs that pass the same specification requirements.

Looking at eye height, on the other hand, we see real problems with reduction in the logical high voltage level as eye height decreases. With 90% emitter resistance mismatch the eye height can be reduced by 20%. In theory, this could bring a signal swing from 1V down to 800mV. This design uses a high voltage level of 2mV, which can drop down past 1.6mV with 90% emitter resistance mismatch.

	Delta RC	Delta Beta	Delta RE
% mismatch	85%	N/A	85%
High Voltage Level	1.8mV	N/A	1.62mV
High Voltage Level Decrease	0.2mV	N/A	0.38mV
Decrease %	10%	N/A	19%

Table 4.6: High Voltage Level vs Mismatch

Table 4.6 above summarizes the rough effects of mismatch on high voltage level. As beta mismatch didn't affect eye height in any measurable way for this thesis, it also does not have a real effect on high voltage level. As mismatch increases, it has already been shown that eye height decreases.

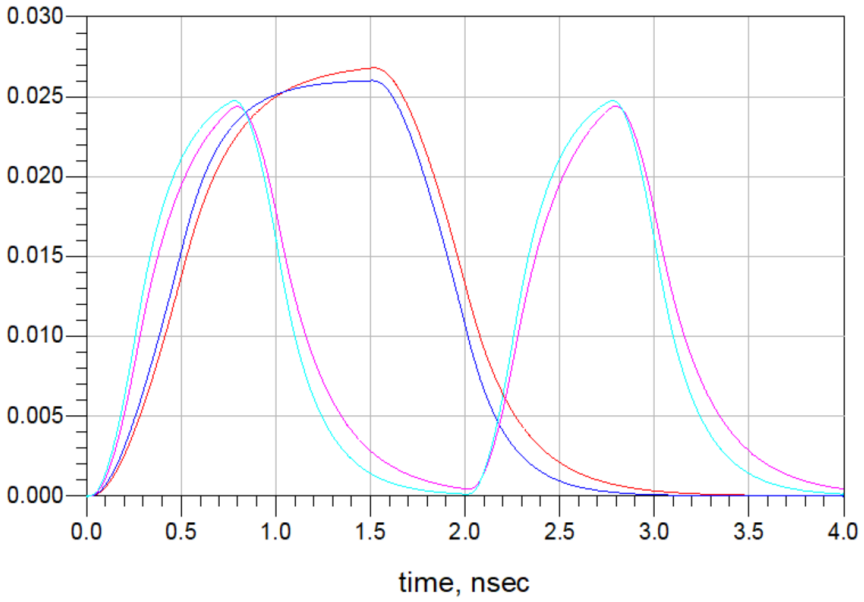

Figure 4.28: 250MHz vs 500MHz Clock Signal Degradation

A more practical explanation of this is reduction in the logical high voltage level. With the high voltage level decreasing, a digital signal can run into errors distinguishing or detecting the high, or “one”, voltage levels and the 1 bit. This can be entirely detrimental to the signal fidelity and the bit error rate. Figure 4.28 above shows the mismatch from Table 4.6 at both frequencies. It can be clearly seen that, at 500MHz in teal and pink, this increased rise time reduces the “hold” time to effectively zero, almost to the point of not reaching the required high voltage level. This effect will be illustrated one step further in the following section.

4.3.6 Mismatch at Higher Frequencies

The final piece of interest in this thesis is how all of these mismatch effects change as a function of frequency. This experiment was performed at 250MHz, which is quite slow in the year 2022 with IC technology surpassing 100GHz. The simulation from above was briefly performed at double the frequency, 500MHz, to gage the effect on rise time. The rise and fall time results with mismatch at 500MHz were surprisingly similar to

at 250MHz. That is to say, the rise and fall times were not halved with the period. Assuming a required up/hold time of 200ps, emitter and collector resistance mismatch on the order of 75% can quickly begin to remove any high/one bit resolution and distinction, effectively rendering the clock signal useless. This suggests an exponential relationship between mismatch effect and operating frequency. To briefly prove this, the simulation done previously was repeated for emitter resistance mismatch effect on rise time at 500MHz.

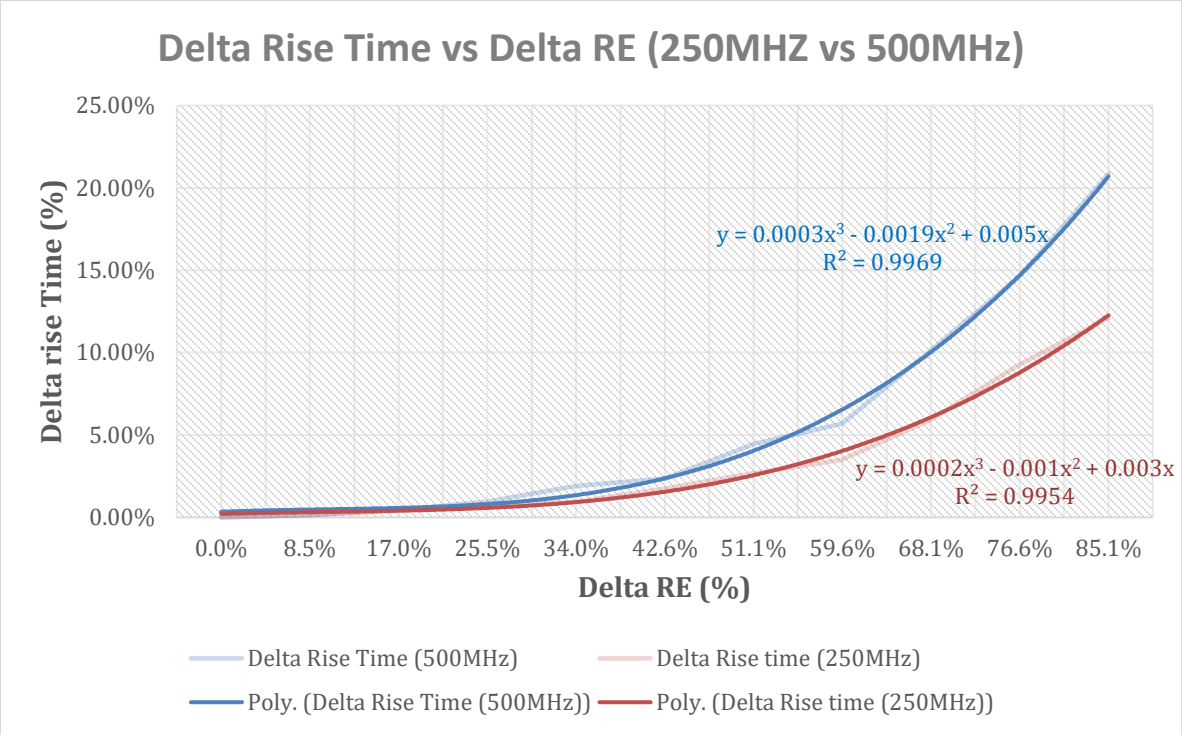

Figure 4.29: Delta Rise Time vs Delta RE (250MHz vs 500MHz)

Figure 4.28 above shows the effect of emitter resistance mismatch on change in rise time at both 250MHz and 500MHz. It can be clearly seen from this plot that rise time is more impacted by emitter resistance mismatch at higher frequency.

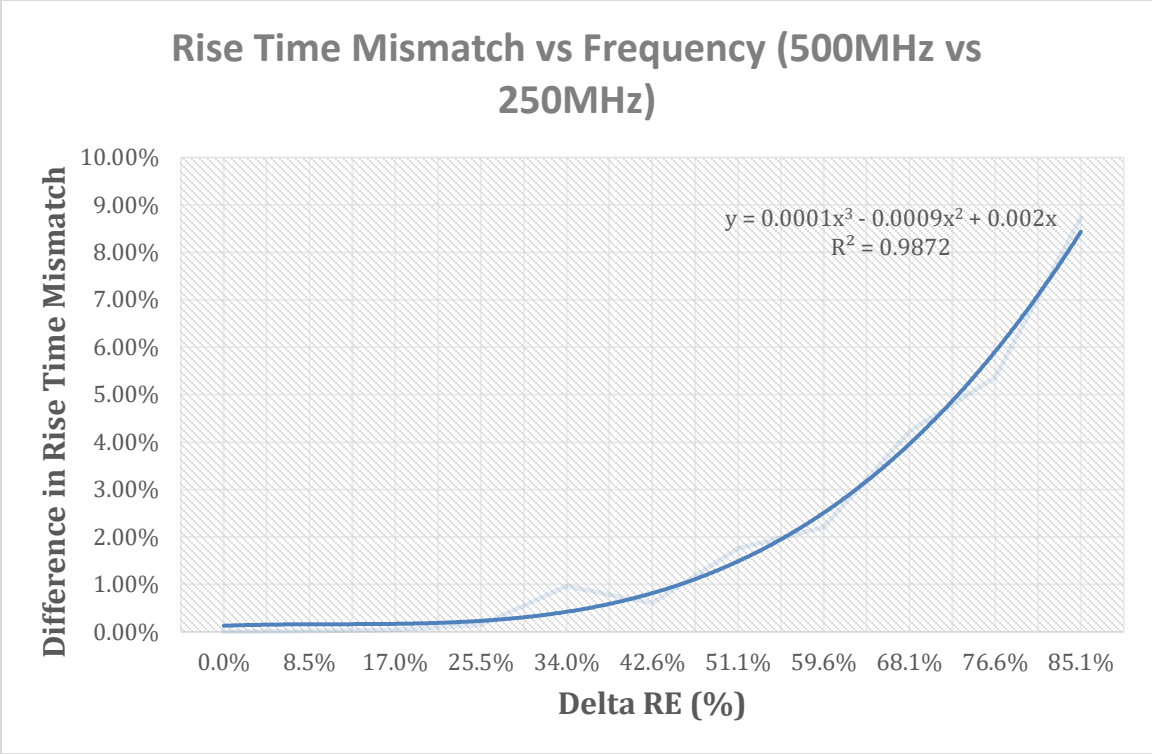

Figure 4.30: 250MHz vs 500MHz Mismatch Difference

Taking this data one step further, at the risk of increased confusion in pursuit of more data presentation, Figure 4.29 above plots the difference between the 250MHz and 500MHz mismatch plots from above.

CHAPTER 5 CONCLUSION

This thesis set out to characterize the effects of general mismatch between two amplifiers on two halves of a differential signal, as measured by use of an eye diagram. The question to be answered was general, as there is shockingly little current research on this topic. As can be seen in a time-interleaved analog-to-digital data converter, parallel signal paths being processed or amplified individually and separately is of new relevance in the field of mismatch characterization, primarily as a direct result of increasing frequency and speed requirements in circuit design. The simple purpose of this thesis, therefore, was to determine whether or not mismatch effects could be directly characterized and quantified in any relevant way by use of an eye diagram.

In the case of a differential digital clock signal, mismatch in general between the individual amplifiers on each half of the signal has been found in this thesis to have predictable and measurable effects on signal fidelity and speed in the eye diagram measurement. As the resistances at the collector and emitter of parallel transistors become less carefully matched, the resulting differential signal at the output is also less well matched between the two halves. If a differential digital clock signal is being used to properly time something like a sampler or a set of analog-to-digital converters, for example, errors in the fidelity of these timing bits can easily cause significant performance issues. In addition, as frequency increases, these issues could only be effectively detected at the outputs of the devices being clocked, making it potentially far more difficult to diagnose failure cause. This increases the likelihood of accidentally replacing perfectly functional components under the assumption they are failing, when the real issue could be errors and mismatch on the clock signal.

	Delta RC	Delta Beta	Delta RE
% mismatch	25%	N/A	25%
Delta Eye Height	1%	N/A	1%
% mismatch	50%	N/A	10%
Delta Rise Time	1%	N/A	1%
% mismatch	10%	20%	25%
Delta SNR	1%	0%	1%

Table 5.1: Mismatch Tolerances

Table 5.1 above shows the tolerances in mismatch of collector resistance, emitter resistance, and beta and their effects on changes in eye height, rise time, and signal-to-noise ratio for this parallel amplifier configuration. The greatest correlations found in this thesis and for this configuration were 10% to 1%, for ΔR_C – ΔSNR and ΔR_E – ΔRiseTime.

A far more practical explanation of the eye height reductions is the reduction of the logical high voltage level as a result of mismatch. As the signal fails to reach the specified high voltage level, 2mV in this design, the system encounters greater difficulties detecting the “1” bits in the signal. As mismatch increases, bit error rate can also increase for a digital clock signal.

In addition, this thesis was able to loosely verify an exponential relationship between mismatch results and operating frequency.

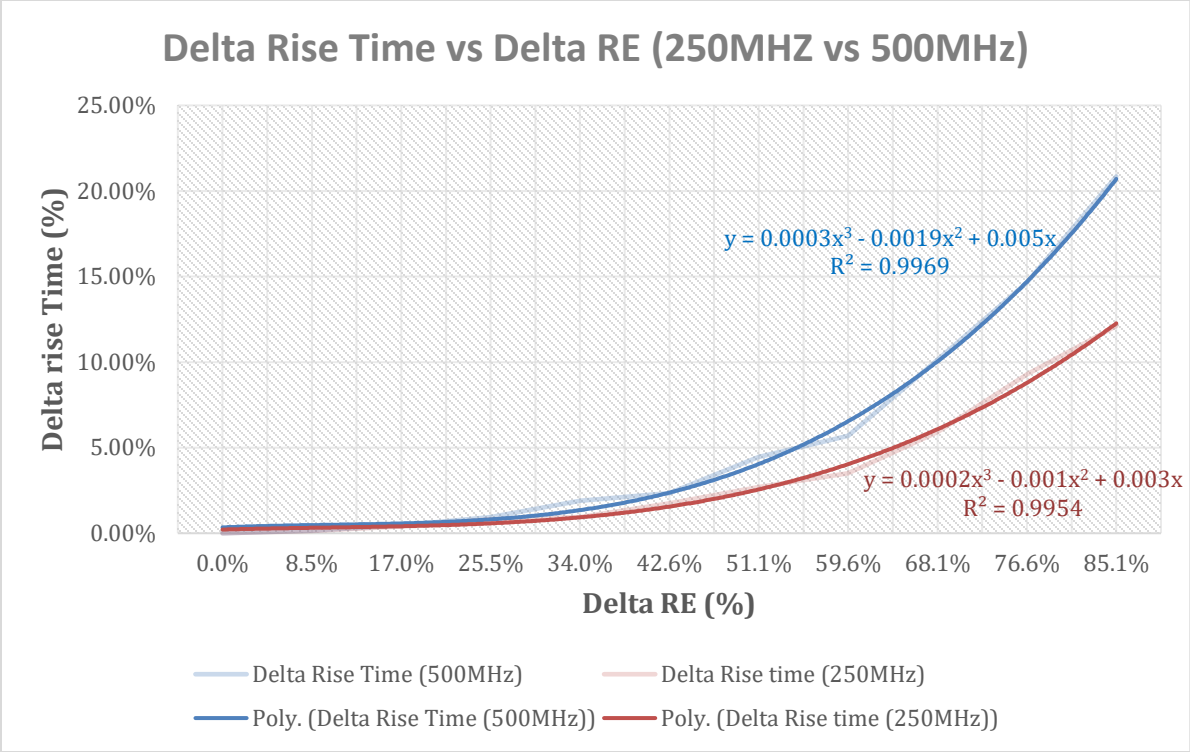

Figure 5.1: Delta Rise Time vs Delta RE (250MHz vs 500MHz)

While 200% emitter resistance mismatch is not enough to remove the hold/up time at 250MHz, any hold time is completely removed as a result of only 75% emitter resistance mismatch at 500MHz. Figure 5.1 above from the results section shows a startlingly clear correlation between mismatch effects and operating frequency.

The model developed and utilized in this thesis was verified to be a reasonably accurate representation of real circuit behavior when its rise time signal was compared to that of the simulation.

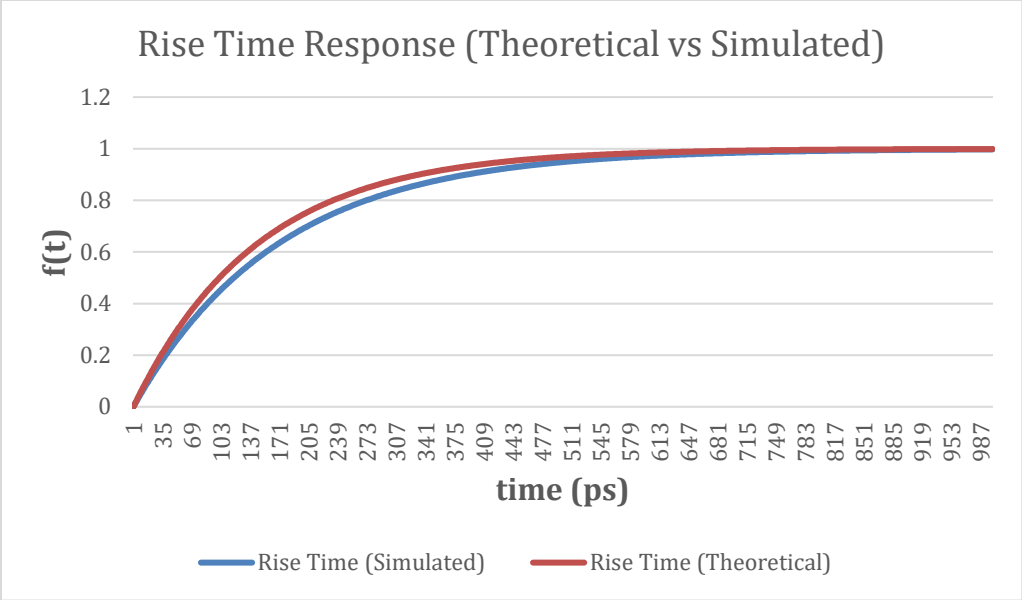

Figure 5.2: Model Accuracy Verification

As frequency and performance demands become faster and tighter, this differential signal mismatch may become far more common and detrimental. Further research is needed to identify and characterize how the effects of this type of mismatch worsen as signal frequency increases. While this thesis investigated this effect briefly at 500MHz, another useful experiment would be a more broadband amplifier design that could sweep at frequencies far into the gigahertz range. In addition, to better understand the finer points of the effects of mismatch, it would be prudent to design and build multiple physical amplifier circuits using on paper “identical” transistors and components. These circuits could be connected in parallel to a differential signal and the outputs measured using an eye diagram on an oscilloscope. The expectation is that the correlation between percent change in device parameters and output signal fidelity and matching will be even stronger with real-world inconsistencies and process variations.

REFERENCES

Asenov, A., Brown, A. R., Davies, J. H., Kaya, S., & Slavcheva, G. (2003). Simulation of intrinsic parameter fluctuations in decananometer and nanometer-scale MOSFETs. *IEEE Transactions on Electron Devices*, *50*(9), Article 9. https://doi.org/10.1109/TED.2003.815862

Asenov, A., Kaya, S., & Davies, J. H. (2002). Intrinsic threshold voltage fluctuations in decanano MOSFETs due to local oxide thickness variations. *IEEE Transactions on Electron Devices*, *49*(1), Article 1. https://doi.org/10.1109/16.974757

Bogatin, E. (2018, May 14). *Back to Basics: Bandwidth and Rise Time*. Signal Integrity Journal. https://www.signalintegrityjournal.com/blogs/12-fundamentals/post/853-back-to-basics-bandwidth-and-rise-time

Carusone, T. C., Johns, D. A., & Martin, K. W. (2011). *Analog Integrated Circuit Design* (Second). John Wiley & Sons.

Cheng, Q., Li, W., Tang, X., & Guo, J. (2019). Design and Analysis of Three-Stage Amplifier for Driving pF-to-nF Capacitive Load Based on Local Q-Factor Control and Cascode Miller Compensation Techniques. *Electronics*, *8*(5), Article 5. https://doi.org/10.3390/electronics8050572

Difrenza, R., Llinares, P., Taupin, S., Palla, R., Garnier, C., & Ghibaudo, G. (n.d.). *Comparison between matching parameters and fluctuations at the wafer level*. 6.

Display eye diagram of time-domain signal—Simulink. (n.d.). Retrieved October 24, 2022, from https://www.mathworks.com/help/comm/ref/eyediagramscope.html

Drennan, P. G., & McAndrew, C. C. (1999). A comprehensive MOSFET mismatch model. *International Electron Devices Meeting 1999. Technical Digest (Cat. No.99CH36318)*, 167–170. https://doi.org/10.1109/IEDM.1999.823871

Drennan, P. G., & McAndrew, C. C. (2003). Understanding MOSFET mismatch for analog design. *IEEE Journal of Solid-State Circuits*, *38*(3), Article 3. https://doi.org/10.1109/JSSC.2002.808305

EDN. (2011, December 16). Eye diagram basics: Reading and applying eye diagrams. *EDN*. https://www.edn.com/eye-diagram-basics-reading-and-applying-eye-diagrams/

Gogolides, E., Constantoudis, V., Patsis, G. P., & Tserepi, A. (2006). A review of line edge roughness and surface nanotexture resulting from patterning processes. *Microelectronic Engineering*, *83*(4–9), 1067–1072. https://doi.org/10.1016/j.mee.2006.01.162

Han, M.-H., Li, Y., & Hwang, C.-H. (2010). The impact of high-frequency characteristics induced by intrinsic parameter fluctuations in nano-MOSFET device and circuit. *Microelectronics Reliability*, *50*(5), Article 5. https://doi.org/10.1016/j.microrel.2010.01.048

Herres, D. (2016, August 16). *The Eye Diagram: What is it and why is it used?* https://www.testandmeasurementtips.com/basics-eye-diagrams/

Lakshmikumar, K. R., Hadaway, R. A., & Copeland, M. A. (n.d.). *Characterisation and modeling of mismatch in MOS transistors for precision analog design*. 10.

Li, Y., & Cheng, H.-W. (2012). Random Work-Function-Induced Threshold Voltage Fluctuation in Metal-Gate MOS Devices by Monte Carlo Simulation. *IEEE Transactions on Semiconductor Manufacturing*, *25*(2), 266–271. https://doi.org/10.1109/TSM.2011.2181964

Line Edge Roughness (LER). (n.d.). Semiconductor Engineering. Retrieved November 11, 2022, from https://semiengineering.com/knowledge_centers/manufacturing/lithography/line-edge-roughness-ler/

Lofstrom, K., Daasch, W. R., & Taylor, D. (2000). IC identification circuit using device mismatch. *2000 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.00CH37056)*, 372–373. https://doi.org/10.1109/ISSCC.2000.839821

Lovett, J., Cllancy, R., Welten, M., Mathewson, A., & Masont, B. (n.d.). *Characterizing the Mismatch of Submicron MOS Transistors*. 4.

Manganaro, G., & Robertson, D. H. (n.d.). *Interleaving ADCs: Unraveling the Mysteries | Analog Devices*. Analog Dialogue. Retrieved November 1, 2022, from https://www.analog.com/en/analog-dialogue/articles/interleaving-adcs.html

Marshall, A. (2009). Mismatch and Noise in Modern IC Processes. *Synthesis Lectures on Digital Circuits and Systems*, *4*(1), Article 1. https://doi.org/10.2200/S00171ED1V01Y200901DCS019

McShane, E. A., & Shenai, K. (2005). *The Electrical Engineering Handbook*. Academic Press.

Ou, N., Farahmand, T., Kuo, A., Tabatabaei, S., & Ivanov, A. (2004). Jitter models for the design and test of Gbps-speed serial interconnects. *IEEE Design Test of Computers*, *21*(4), Article 4. https://doi.org/10.1109/MDT.2004.34

Pelgrom, M. J. M., Duinmaijer, A. C. J., & Welbers, A. P. G. (1989). Matching properties of MOS transistors. *IEEE Journal of Solid-State Circuits*, *24*(5), Article 5. https://doi.org/10.1109/JSSC.1989.572629

Reducing Signal Noise in Practice | Precision Digital. (n.d.). Retrieved October 18, 2022, from https://www.predig.com/whitepaper/reducing-signal-noise-practice

Rodrigues, S., & Bhat, M. S. (2006). Impact of Process Variation Induced Transistor Mismatch on Sense Amplifier Performance. *2006 International Conference on Advanced Computing and Communications*, 497–502. https://doi.org/10.1109/ADCOM.2006.4289943

Sedra, A. S., & Smith, K. C. (2015). *Microelectronic circuits* (Seventh edition). Oxford University Press.

Shyh-Chyi Wong, Kuo-Hua Pan, & Dye-Jyun Ma. (1997). A CMOS mismatch model and scaling effects. *IEEE Electron Device Letters*, *18*(6), Article 6. https://doi.org/10.1109/55.585349

Shyu, J.-B., Temes, G. C., & Yao, K. (1982). Random errors in MOS capacitors. *IEEE Journal of Solid-State Circuits*, *17*(6), Article 6. https://doi.org/10.1109/JSSC.1982.1051862

Storr, W. (2019, March 18). Common Base Amplifier Configuration. *Basic Electronics Tutorials*. https://www.electronics-tutorials.ws/amplifier/common-base-amplifier.html

Suarez, A., Ramirez, F., & Sancho, S. (2015). Generalized Stability Criteria for Power Amplifiers Under Mismatch Effects. *IEEE Transactions on Microwave Theory and Techniques*, *63*(12), Article 12. https://doi.org/10.1109/TMTT.2015.2494578

The Instrumentation Amplifier | Operational Amplifiers | Electronics Textbook. (n.d.). Retrieved October 18, 2022, from https://www.allaboutcircuits.com/textbook/semiconductors/chpt-8/the-instrumentation-amplifier/

Tocci, G. (2010). *Performance estimation and Variability from Random Dopant Fluctuations in junctionless Multi-Gate FETs: A Simulation Study*. 64.

Transistor Gain: HFE hfe & Beta » Electronics Notes. (n.d.). Retrieved July 28, 2022, from https://www.electronics-notes.com/articles/electronic_components/transistor/current-gain-hfe-beta.php

Weste, N. H. E., & Harris, D. M. (2011). *CMOS VLSI design: A circuits and systems perspective* (4th ed). Addison Wesley.

Yiming Li & Chih-Hong Hwang. (2008). High-Frequency Characteristic Fluctuations of Nano-MOSFET Circuit Induced by Random Dopants. *IEEE Transactions on Microwave Theory and Techniques*, *56*(12), Article 12. https://doi.org/10.1109/TMTT.2008.2007077